AD-A077 062 JOHNS HOPKINS UNIV LAUREL MD APPLIED PHYSICS LAB F/G 22/3
NAVPAC -- A SPACE-QUALIFIED NAVIGATION PACKAGE.(U)
FEB 79 D L ZITTERKOPF N00017-72-C-4401
UNCLASSIFIED APL/JHU/TG-1317 NL

1 OF 2
AD A077062

APL/JHU
TG 1317
FEBRUARY 1979
Copy No. 1

LEVEL II

12

Technical Memorandum

NAVPAC—A SPACE-QUALIFIED NAVIGATION PACKAGE

D. L. ZITTERKOPF

THE JOHNS HOPKINS UNIVERSITY ■ APPLIED PHYSICS LABORATORY

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE

PLEASE FOLD BACK IF NOT NEEDED FOR BIBLIOGRAPHIC PURPOSES

REPORT DOCUMENTATION PAGE

1. REPORT NUMBER: APL/JHU TG-1317	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (*and Subtitle*): NAVPAC -- A Space-Qualified Navigation Package	5. TYPE OF REPORT & PERIOD COVERED: Technical Memorandum
6. PERFORMING ORG. REPORT NUMBER: TG 1317	
7. AUTHOR(s): D. L. Zitterkopf	8. CONTRACT OR GRANT NUMBER(s): N00017-72-C-4401
9. PERFORMING ORGANIZATION NAME & ADDRESS: The Johns Hopkins University Applied Physics Laboratory, Johns Hopkins Road, Laurel, MD 20810	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: ZA8
11. CONTROLLING OFFICE NAME & ADDRESS: Defense Mapping Agency, Headquarters, DMA/PRA, Washington, DC 20305	12. REPORT DATE: February 1979 13. NUMBER OF PAGES: 145
14. MONITORING AGENCY NAME & ADDRESS: Naval Plant Representative Office, Johns Hopkins Road, Laurel, MD 20810	15. SECURITY CLASS. (*of this report*): Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (*of this Report*): Approved for public release: distribution unlimited	
17. DISTRIBUTION STATEMENT (*of the abstract entered in Block 20, if different from Report*)	
18. SUPPLEMENTARY NOTES	

19. KEY WORDS (*Continue on reverse side if necessary and identify by block number*)

Atmospheric density studies
Gravity-field analysis
Navy Navigation Satellite System
Phase-locked loop receiver
Spacecraft time annotation
Space-qualified

20. ABSTRACT (*Continue on reverse side if necessary and identify by block number*)

NAVPAC (Navigation Package) is a space-qualified receiver instrument designed and developed by APL for the Defense Mapping Agency. The use of NAVPAC represents the first application of the Navy Navigation Satellite System to reconstruct accurately the orbit of another space vehicle. It also represents the first system for automatically providing a precise time-annotation capability for an event that occurs on a spacecraft.

NAVPAC contains three dual-channel receivers to acquire and track signals automatically from as many as three Navy Navigation Satellites that are in view simultaneously. To help meet the program goals, NAVPAC also includes a three-axis miniature electrostatic accelerometer. The goals of NAVPAC include accurately reconstructing a host-vehicle orbit, providing atmospheric density information, and improving the gravity field model.

DD FORM 1 JAN 73 1473

Unclassified

SECURITY CLASSIFICATION OF THIS PAGE

APL/JHU
TG 1317
FEBRUARY 1979

Technical Memorandum

NAVPAC—A SPACE-QUALIFIED NAVIGATION PACKAGE

D. L. ZITTERKOPF

THE JOHNS HOPKINS UNIVERSITY ■ APPLIED PHYSICS LABORATORY
Johns Hopkins Road, Laurel, Maryland 20810
Operating under Contract N00024-78-C-5384 with the Department of the Navy

ABSTRACT

NAVPAC (Navigation Package) is a space-qualified receiver instrument designed and developed by APL for the Defense Mapping Agency. The use of NAVPAC represents the first application of the Navy Navigation Satellite System to reconstruct accurately the orbit of another space vehicle. It also represents the first system for automatically providing a precise time-annotation capability for an event that occurs on a spacecraft.

NAVPAC contains three dual-channel receivers to acquire and track signals automatically from as many as three Navy Navigation Satellites that are in view simultaneously. To help meet the program goals, NAVPAC also includes a three-axis miniature electrostatic accelerometer. The goals of NAVPAC include accurately reconstructing a host-vehicle orbit, providing atmospheric density information, and improving the gravity field model.

CONTENTS

ILLUSTRATIONS

TABLES

1. INTRODUCTION

The Navigation Package (NAVPAC) is a space-qualified receiver instrument designed and developed by the Applied Physics Laboratory (APL) for the Defense Mapping Agency (DMA). NAVPAC contains three dual-channel receivers to acquire and track signals automatically from as many as three Navy Navigation Satellites that are simultaneously in view. The goals of NAVPAC include accurately reconstructing a host-vehicle (HV) orbit, providing atmospheric-density information, and improving the gravity-field model. To help meet the program goals, NAVPAC includes a three-axis miniature electrostatic accelerometer (MESA) developed by the Bell Aerospace Corporation to sense all nongravitational accelerations of the space vehicle.

The NAVPAC data system collects and temporarily stores all instrument data in a buffer prior to storage on a tape recorder. After several blocks of data have been stored on the tape recorder, the data are transmitted to a ground station via a host-vehicle data link. All data will be used at the Naval Surface Weapons Center (NSWC), Dahlgren, Virginia, to reconstruct the orbit of the host vehicle and refine the gravity field model of the earth. The Air Force Geophysics Laboratory will use the MESA data for atmospheric density studies.

NAVPAC can be commanded into several configurations from oscillator-only on to all-systems on. In addition, the buffer storage allocated to the various data types can be modified by command, allowing maximum flexibility if power constraints are imposed during the mission, or if part of NAVPAC fails.

2. FUNCTIONAL DESCRIPTION

NAVPAC (Fig. 1) consists of two sensing systems (the multisatellite receiver and the accelerometer) and associated control and data processing hardware. The subject matter of this report is limited to the equipment developed by APL and therefore excludes MESA, which is mounted remotely from the receiver/data system and is connected by an externally routed cable.

To meet program goals, the system was designed with the following characteristics:

1. The antenna must be capable of receiving 400-MHz signals with left-hand or right-hand circular polarization, and 150-MHz signals with left-hand circular polarization.

2. The receiver must be capable of acquiring and tracking signal sets from as many as three Navy Navigation Satellites (NAVSAT) simultaneously.

3. The data system must collect, time annotate, and buffer all data prior to data storage by tape recorder.

4. The data system must provide time annotation of the occurrence of external (to NAVPAC) event signals.

5. A power conditioning unit (DC/DC converter) must convert the raw power from the space vehicle to the various voltages required by the receiver/data system.

The antenna is launched in a stowed position and is deployed vertically by a mechanism provided by a host vehicle. The antenna system consists of a 400-MHz dipole and a left-hand circularly polarized quadrifilar helix for 150-MHz reception, both mounted on a common boom. The 400-MHz dipole allows reception of the left- and right-hand circularly polarized signals transmitted by the various NAVSATs in orbit.

The multisatellite receiver consists of a frequency synthesizer, three dual-channel (i.e., two-frequency) phase-locked tracking loops (DTL) with associated control logic, and two RF sections. Each RF section contains a narrowband preselection filter, preamplifier, and IF amplifier. The system requirements of the receiver include:

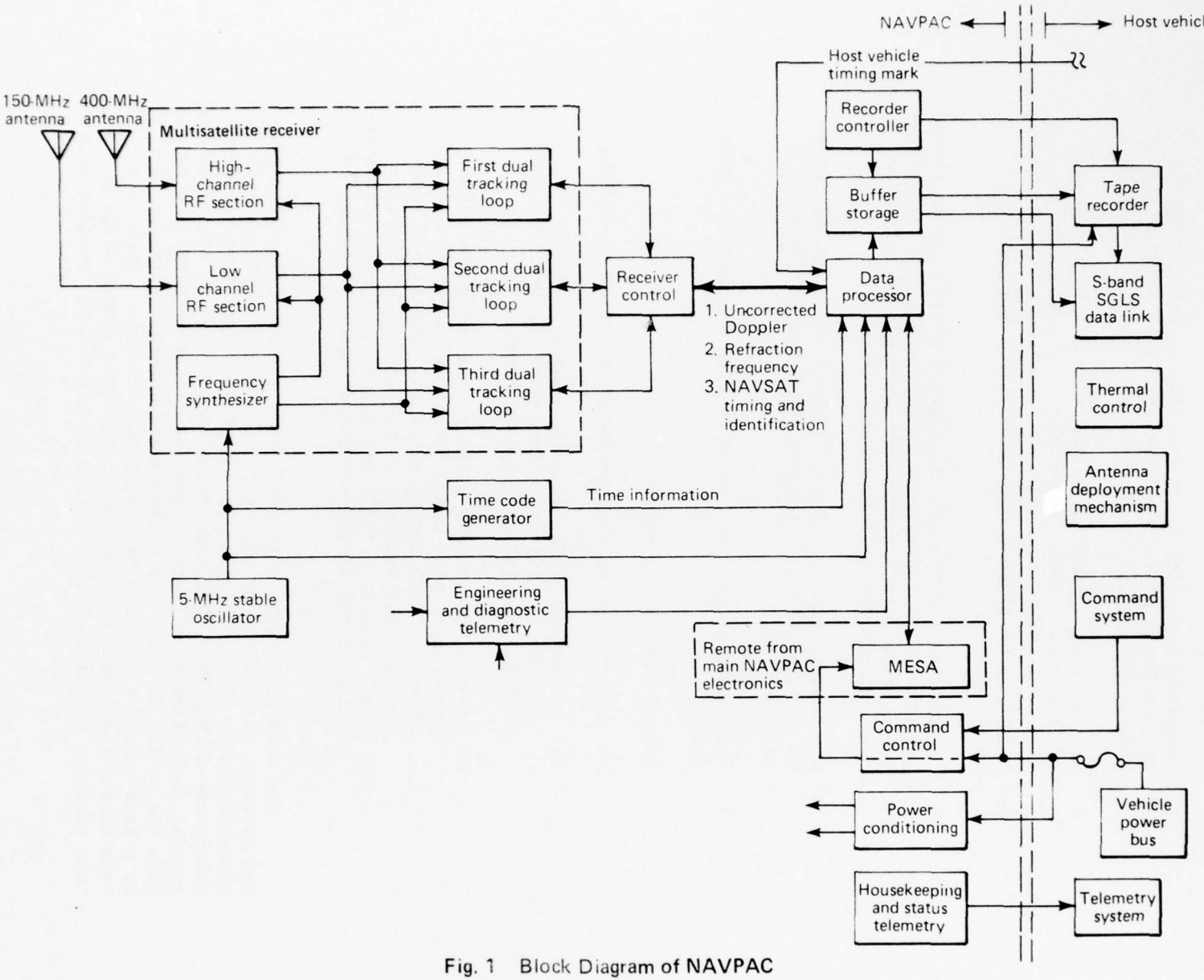


Fig. 1 Block Diagram of NAVPAC

1. Automatic acquisition and tracking of NAVSAT signals without "pass alert" information (i.e., predictions of when a NAVSAT will be in view, as a function of time);

2. Automatic reacquisition of the signal being tracked after a signal fade (e.g., due to an antenna null);

3. Rejection of signals that do not have NAVSAT-type modulation;

4. Acquisition and tracking of signals whose Doppler characteristics (i.e., frequency rate-of-change and total frequency rise-to-set excursion) are approximately twice that observed by a fixed ground station;

5. Acquisition and tracking of signals at elevations down to -10°, relative to the horizon plane of the host vehicle; and

6. Prevention of any two DTL units from tracking the same NAVSAT.

7. Output signals representing

   a. uncorrected Doppler frequency referred to 400 MHz,

   b. ionospheric refraction information referred to 400 MHz (a difference frequency derived from the 400-MHz and 150-MHz signals), and

   c. demodulated NAVSAT signals from which the NAVSAT two-minute time marks (TMTM) and satellite identification (ID) can be obtained. The NAVSAT time marks allow calibration of the data system time code generator (TCG) and are also required for solution of the navigation computations performed by NSWC.

The data processing unit (DPU) controls all data collection and movement in NAVPAC. At the heart of the DPU is the central processing unit (CPU), which accepts digitized data from various subsystems of the DPU. The function of the CPU is to create several special data files of different types of data in a temporary buffer. When the buffer is full, its contents are automatically transferred to a tape recorder that can hold many buffer dumps. Much later, the tape recorder contents can be transmitted to a ground station. A tape recorder bypass mode also exists to allow data transfer directly

from the buffer to the ground station in the event that the recorder fails. The CPU accepts data from the TCG (a counter driven by an ultrastable 5-MHz oscillator to create a precision time annotation mechanism), the MESA, the Doppler and refraction counters for the three DTL units, the NAVSAT TMTM and ID-recovery electronics, and the engineering and diagnostic telemetry electronics.

The DC/DC converter converts the host-vehicle unregulated power bus into the various voltages needed by the receiver and data systems. A switching-down regulator is used to preregulate the bus into a Jensen converter. A switching regulator was chosen for its inherent high efficiency, an item of prime importance. The converter is sized for maximum efficiency at the normal expected load.

3. PHYSICAL DESCRIPTION

WEIGHT, VOLUME, AND POWER

Weight and volume were not limiting factors in the initial NAVPAC design, but schedule was; therefore, the system was packaged in the most expedient (not necessarily the smallest or minimum-weight) configuration. Packages for the multisatellite receiver, the data system, and associated electronic modules are mounted on a 28 in. x 46 in. baseplate (Fig. 2) with a maximum height of 10 in. The panel assembly weighs approximately 134 lb. The antenna envelope is a cylinder, 8.5 in. in diameter and 64 in. long (Fig. 3). This assembly weighs 4.5 lb, not including the deployment mechanism.

The NAVPAC electronics requires 16 W from a +28-VDC bus. To minimize power consumption, extensive use was made of COSMOS* devices for the logic design in the data system and the receiver control electronics.

ELECTRONIC PACKAGING TECHNIQUES

In order to reduce design time and costs, several fabrication and packaging techniques were used for NAVPAC that were a major departure from "typical" spaceflight-hardware techniques. These techniques included: (a) use of dual in-line integrated circuits mounted on plug-in boards with point-to-point back plane wirewrap interconnects and (b) use of extruded aluminum boxes for enclosures for most of the electronics. Standard printed circuit construction techniques were used for items such as the frequency synthesizer, all RF assemblies, and the DC/DC converter.

WEIGHT AND VOLUME REDUCTION POSSIBILITIES

Reduction of the weight and volume of the NAVPAC electronics has been considered. Except for items such as the dual oscillator, the DC/DC converter, the antenna, and preselect filters, it is believed that the package volume could be reduced to perhaps 50% or even 25% of the volume that the electronics now represent. Because the chassis represents a large percentage of the weight of each module, the package weight would tend to decrease linearly with volume.

---

* RCA trade name for complementary symmetrical metal oxide semiconductor.

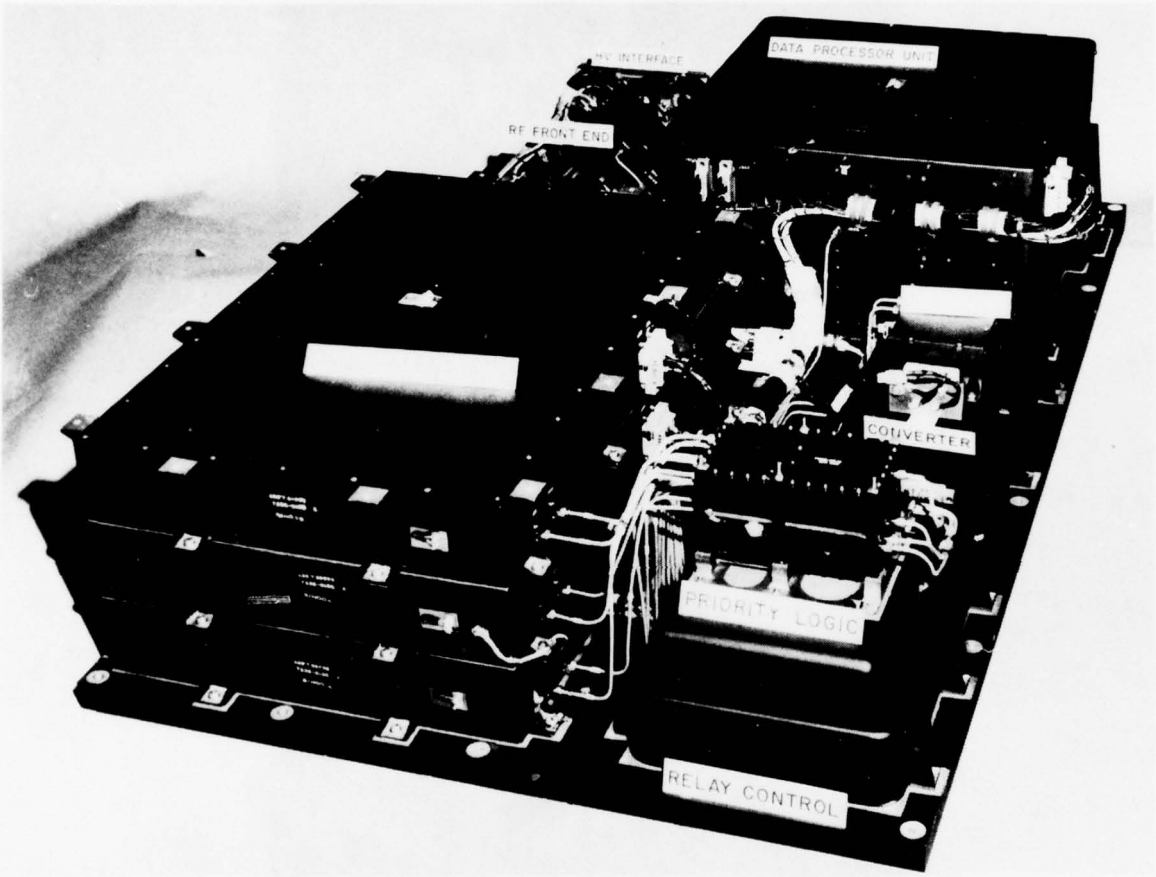


Fig. 2 NAVPAC Data System and its Associated Electronics

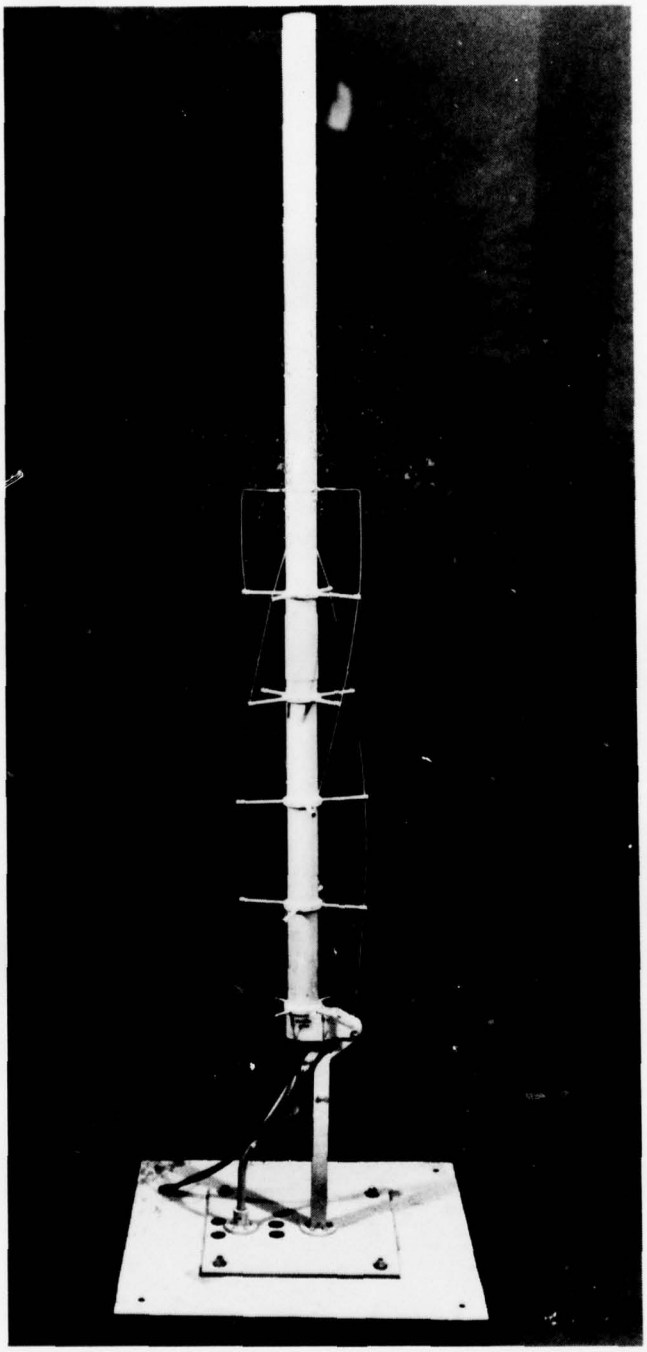


Fig. 3 NAVPAC Antenna, Showing the 150-MHz Quadrifilar Helix and the 400-MHz Vertical Dipole

4. TESTING

SUBSYSTEM TESTING

Before the individual pieces of the multisatellite receiver, the data processing unit, the oscillator, the power-conditioning unit, and the relay package were integrated on the flight panel, they were subjected to tests of three-axis random vibration and temperature and input-voltage stress. The oscillator and power conditioning unit were tested in a thermal-vacuum chamber because of their particular design characteristics, but the other components were tested in temperature chambers.

SYSTEM TESTING BEFORE SHIPMENT TO THE FIELD

The components of the NAVPAC were integrated onto the panel serially. After the initial checkout of the panel wiring harness, the power-conditioning unit was installed and powered. The relay package was then installed and the power-distribution wiring was confirmed. The multisatellite receiver, oscillator, and DPU were then installed and power applied to begin the initial complete test at the system level.

System testing of NAVPAC was segmented into a group of individual specialized tests that included tests of receiver acquisition and drop-lock, navigation message and time-recovery, DPU files, TCG, telemetry, oscillator stability, and so on. (The individual test sequences became the basis for tests performed at the host-vehicle integration contractor (HVIC) facilities.) Conducting the tests and processing and recording the data were semiautomated by a dedicated minicomputer that typed test instructions to the test conductor and then processed and displayed the resultant data in accordance with the preplanned test sequences.

After proper working of the system was assured, an antenna/preamplifier assembly mounted on the roof of the test area was used to collect the same type of Doppler data from NAVSATs as will occur when NAVPAC is in orbit. The data were stored on a tape recorder each time there was a data-processor buffer dump. The data were then processed by NSWC. In order to gain experience with the quality of data that NAVPAC would produce, many hours of data of this type were collected in each of the various NAVPAC modes.

The MESA package was interfaced to NAVPAC to determine whether there were any problems between the two devices. No such problem was observed, and the interface test was successful.

The entire panel (minus MESA) was then installed in the APL thermal/vacuum chamber and subjected to a series of hot-cold cycles and soak periods. During those periods, NAVPAC was tested according to the standard test sequences and additional satellite tracking data were recorded, using the flight oscillator. (The previous room-temperature tracking data were obtained using a laboratory standard oscillator because the flight oscillator will not provide a stable reference signal unless it is in a vacuum.)

After the thermal/vacuum test was completed, NAVPAC was taken to an EMC test facility. There the program included testing of the NAVPAC susceptibility to external radiation and susceptibility to external interference conducted on the power and signal leads. Also, tests were conducted to determine what interference the NAVPAC emitted on power and signal lines and what interference it radiates. These tests were performed in accordance with Mil-Std-826A. Except for some additional satellite tracking tests and measurement of mass properties, the EMC tests concluded the basic "preship" test sequence and the unit was shipped to the facilities of the HVIC.

SYSTEM TESTING AT THE INTEGRATION CONTRACTOR

Testing at the HVIC facilities consisted of two basic sequences: an initial receiving and inspection (R & I) test (including a pyrotechnic shock test for System 01) controlled and performed by APL personnel, and the module test lab sequence during which NAVPAC was interfaced to the local facilities and simulators provided by the HVIC.

During R & I the sequences originally performed at APL were repeated and the data were compared with the results that were obtained before shipment. Additional satellite tracking tests were performed using an APL-supplied antenna/preamplifier assembly mounted on the roof of the test area. The pyrotechnic shock test was performed and the initial R & I test sequences were repeated. Additional satellite tracking data were also collected. These data were analyzed and the determination was made that the R & I test sequences had been successfully completed.

An acoustic-environment test (instead of a mechanical-displacement vibration test as was performed at APL) and a thermal/vacuum test were performed in the module test laboratory. NAVPAC

was successfully tested before and after the acoustic environment test and was monitored during that test without any change in performance. During the soak periods and hot-cold cycles of the thermal/vacuum test that followed, NAVPAC was repeatedly tested using the basic sequences originally developed at APL. The successful completion of the thermal/vacuum test completed the NAVPAC test program.

5. RESULTS, PERFORMANCE, AND FUTURE PLANS

Prior to shipment of System 01 from APL to the HVIC, extensive NAVSAT tracking data were obtained using a fixed site antenna. The data were recorded under a variety of conditions ranging from room conditions while using a laboratory standard oscillator to high- and low-temperature conditions during thermal-vacuum testing while using the actual flight oscillator. The following results were consistently obtained:

Clock calibration error	<35 μs rms
Average filtered range noise	10 to 15 cm
Navigation consistency	1.7 to 3.5 m

Tables 1 and 2 summarize the processed results obtained by NSWC for some of the data tapes made during the tracking tests. Figure 4 is a plot of slant-range and in-track navigation errors for data tape 18. The average errors were 1.8 m slant range and 0.3 m along-track. This was typical of all the data collected.

System 01, launched during the second quarter of CY 1977, functioned flawlessly. In-orbit results processed by NSWC compared well with the data obtained prior to launch.

Systems 02 and 03 have been delivered to the HVIC. System integration and performance verification of System 04 is being completed at APL. The hardware for Systems 05 and 06 is in the package test and assembly phase. It is estimated that all work at APL will be completed during the first quarter of 1978. There are no current plans for fabricating additional systems.

Table 1

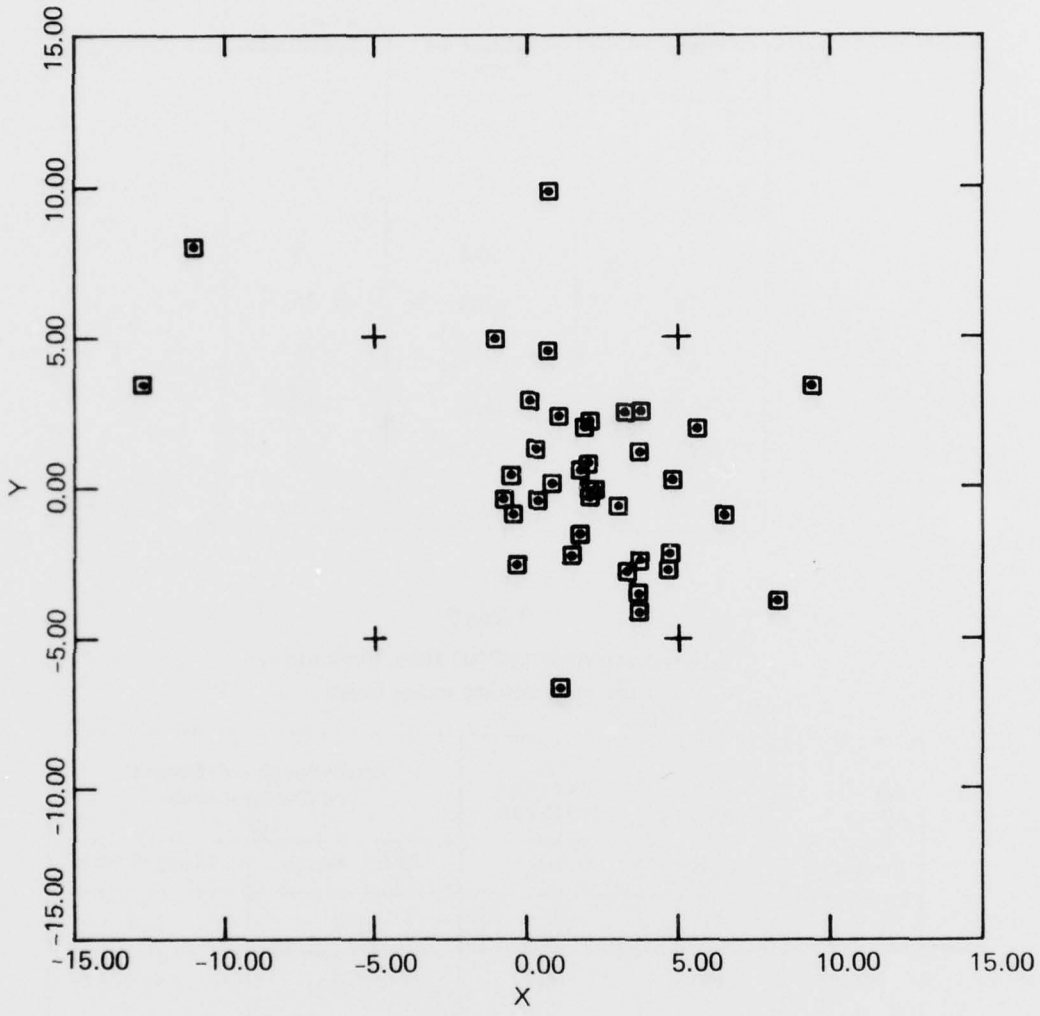
Summary of NAVPAC Clock Calibration

NSWC/DL Data Tape Number	Number of TMTM's	Root-Mean Square of Residuals (μs)
2	442	23
2 (Rec 1 only)	140	15
7	165	33
8	267	28
12	89	25
15	135	33
16	148	34
18	341	31

Table 2

Summary of NAVPAC Data Evaluation (normal tracking mode only)

NSWC/DL Data Tape Number	Number of Passes	Average Filtered Noise (cm)	Root-Weighted-Square of Navigations (m)	
			Slant Range	Along-Track
2	57	10.5	2.8	2.3
7	25	9.9	2.6	2.7
8	35	10.6	3.5	1.9
10	27	13.4	2.3	2.5
12	9	14.9	2.4	2.3
15	15	12.3	2.0	1.7
16	21	13.9	1.7	3.2
18	40	12.6	1.8	2.6



THE X AXIS IS THE SLANT RANGE NAVIGATION
IN METER UNITS

THE Y AXIS IS THE IN TRACK NAVIGATION
IN METER UNITS

Fig. 4 Navigation Results on Data Tape 18

6. MULTISATELLITE RECEIVER

GENERAL DISCUSSION

The multisatellite receiver (Fig. 5) includes an ultrastable reference oscillator, a frequency synthesizer, separate antennas for 150-MHz and 400-MHz reception, low insertion loss and narrow-bandpass preselect filters used with low-noise preamplifiers at 150 MHz and 400 MHz, a high-channel (for 400-MHz signals) first IF amplifier, a low-channel (for 150-MHz signals) first IF amplifier, a Priority Assignment and Frequency Coherency assembly, and three dual-channel (i.e., two-frequency) phase-locked tracking loops, each of which receives signals from the high- and low-channel first IF amplifiers.

Because the receiver must receive signals from as many as three NAVSATs that are simultaneously in view, no AGC is used in the preamplifiers or first IF amplifiers. The combination of a preamplifier, a first IF amplifier, and one-half of a single dual tracking loop (DTL) represents a basic double-heterodyne phase-locked loop receiver. Each DTL is configured as a master/slave in that the channel assigned to 400-MHz tracks the full Doppler dynamics of the received 400-MHz signal and generates a reference signal representing the effect of Doppler at 150 MHz for use by the 150-MHz channel. The 400-MHz channel is called the master, and the 150-MHz channel is the slave. Because of the master/slave interactions, the low-frequency channel of the DTL must only track the signal dynamics caused by ionospheric effects.

Each DTL has independent search and acquisition logic. A separate set of electronics monitors each DTL and prevents any two DTL's from tracking the same NAVSAT. The same electronics assigns priority to the DTL units, as they acquire signals, to determine which DTL should begin a new search pattern when two begin tracking the same signal. Outputs from each DTL include Doppler and refraction signals referred to 400 MHz and the NAVSAT message data used to recover NAVSAT timing and identification data. These signals are processed and stored by the data system as raw Doppler and refraction information.

The high and low channels of each DTL are designed to acquire signals automatically at levels of approximately (but perhaps less than) -138 dBm over the entire ±20-kHz Doppler region, and they will remain locked at levels of approximately (but perhaps less than) -145 dBm over a 0° to +50°C temperature range and voltage variations of ±10%.

ANTENNA

The antenna consists of a 150-MHz quadrifilar helix and a 400-MHz vertical dipole. The design fulfills the goal of providing adequate gain for signals from all NAVSATs now in orbit.

Receiving signals from NAVSATs at 400 MHz presented some difficulty because at that frequency, some of the NAVSATs radiate opposite circular polarizations. After considering a design using two oppositely polarized quadrifilar helixes, a linear antenna design was chosen. The linear antenna (a vertical dipole) offers considerable simplicity over the two-helix design and yet provides enough gain on the horizon to meet the design goal.

Since the NAVSATs radiate the same polarization at 150 MHz, a single quadrifilar helix was used. As shown in Fig. 3, the 150-MHz helix is mounted below the 400-MHz dipole. The antenna is a structurally sound unit because of the fiberglass center-support tube. The feed baluns and matching networks for both antennas are mounted inside the center tube. The entire antenna fits inside an 8.2-in. diameter cylinder, 61.5 in. long.

Electrical Characteristics

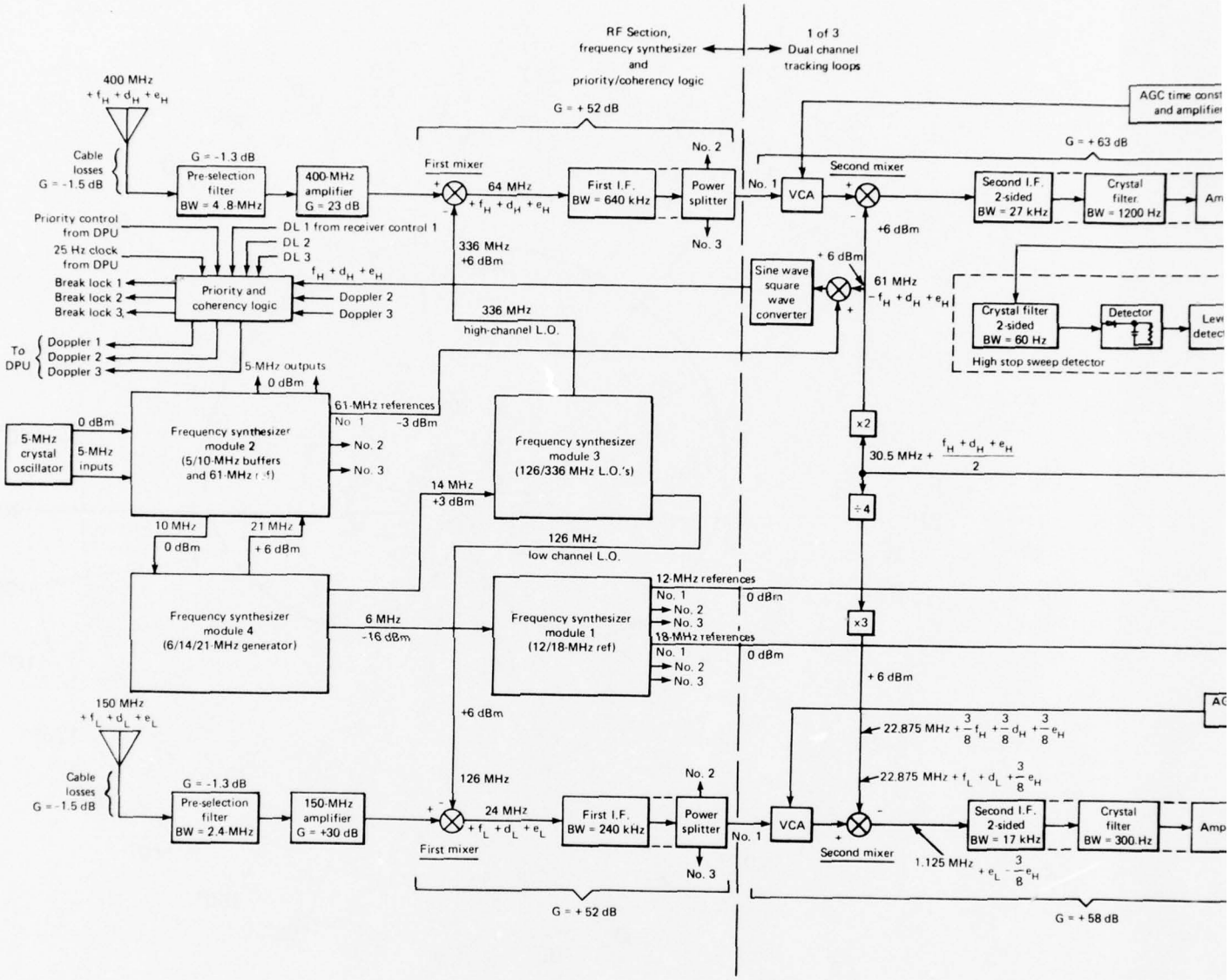
The 150-MHz antenna provides a cardioid radiation pattern as shown in Fig. 6. The antenna is a $\lambda/2$, 3/8-turn left-hand circular volute that has a beamwidth of about 200°.

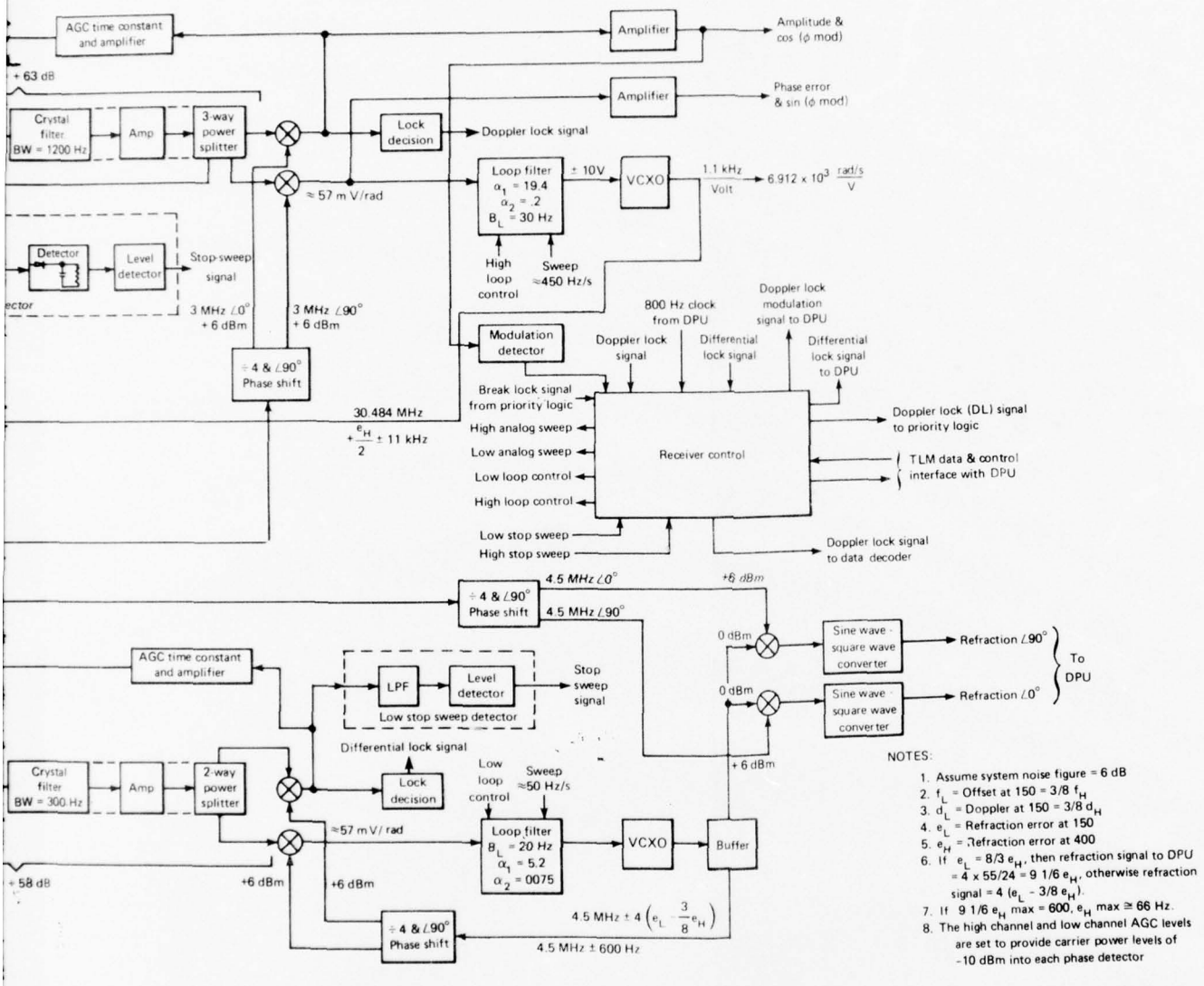
The 400-MHz antenna is a $3\lambda/4$ dipole fed off center to produce the pattern shown in Fig. 7. The beamwidth is about 70° and the beam maximum is shifted 15° toward the long antenna element. This shift is away from the vehicle. A third antenna element (a choke) is positioned below the dipole elements to eliminate any currents from the outside of the feed line. The "overhead" null at 0° does not represent any major system problem, but it does result in momentary loss of signal during a high-elevation pass.

Feed Configuration

Figure 8 shows the feed configuration of the two antennas. The 150-MHz helix is fed by a single folded balun having an extra center tube that provides shielding for the 400-MHz coaxial feed. The extensions from the two balun tubes in the 150-MHz feed region provide the center conductor jumper and give the feed region symmetry.

THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
LAUREL, MARYLAND





NOTES:

1. Assume system noise figure = 6 dB
2. f_L = Offset at 150 = 3/8 f_H
3. d_L = Doppler at 150 = 3/8 d_H
4. e_L = Refraction error at 150
5. e_H = Refraction error at 400
6. If $e_L = 8/3\ e_H$, then refraction signal to DPU = 4 x 55/24 = 9 1/6 e_H, otherwise refraction signal = 4 (e_L - 3/8 e_H).
7. If 9 1/6 e_H max = 600, e_H max ≥ 66 Hz.
8. The high channel and low channel AGC levels are set to provide carrier power levels of -10 dBm into each phase detector

Fig. 5 Block Diagram of the NAVPAC Receiver

2

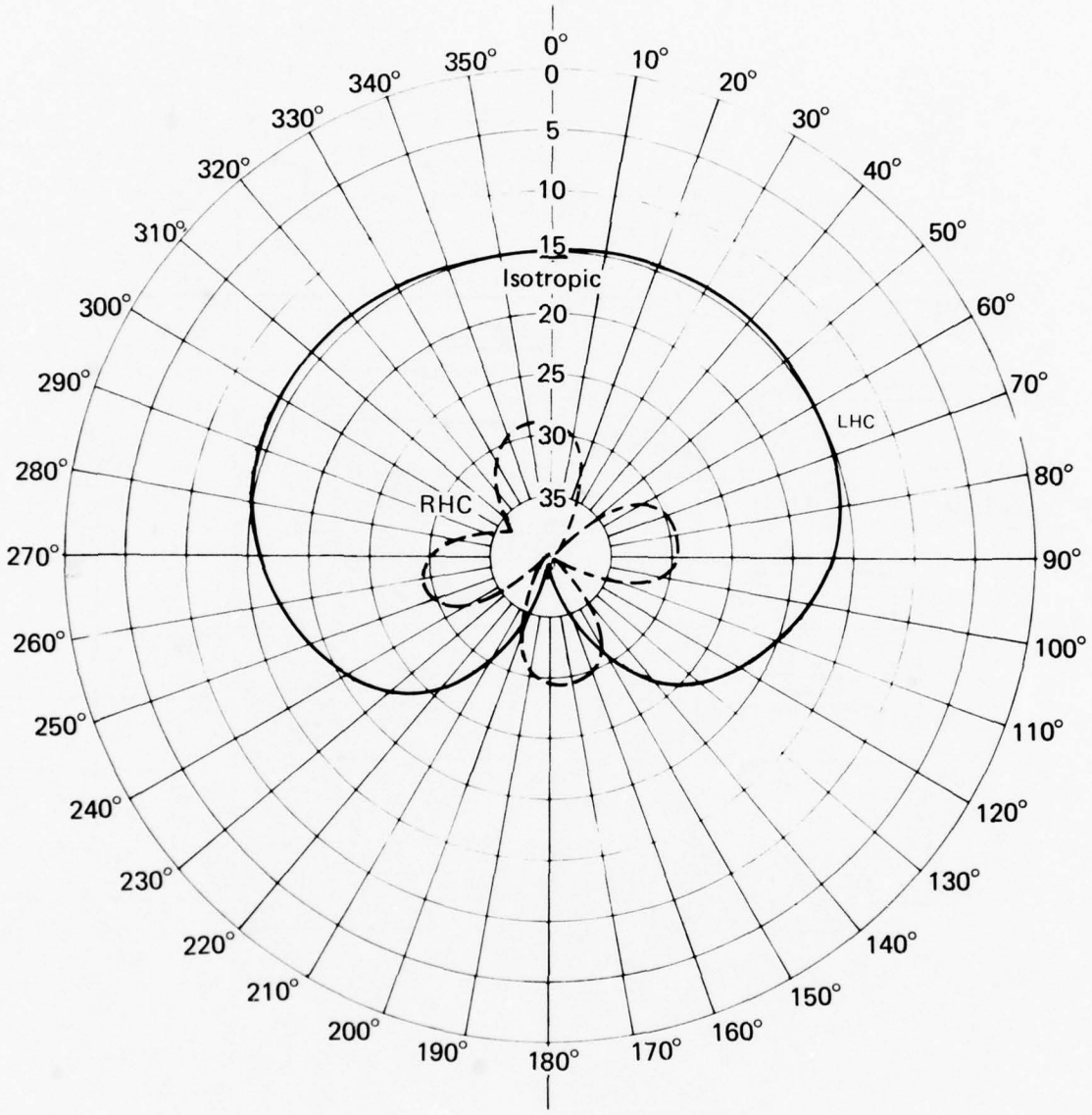


Fig. 6 Radiation Pattern of the 150-MHz Helix

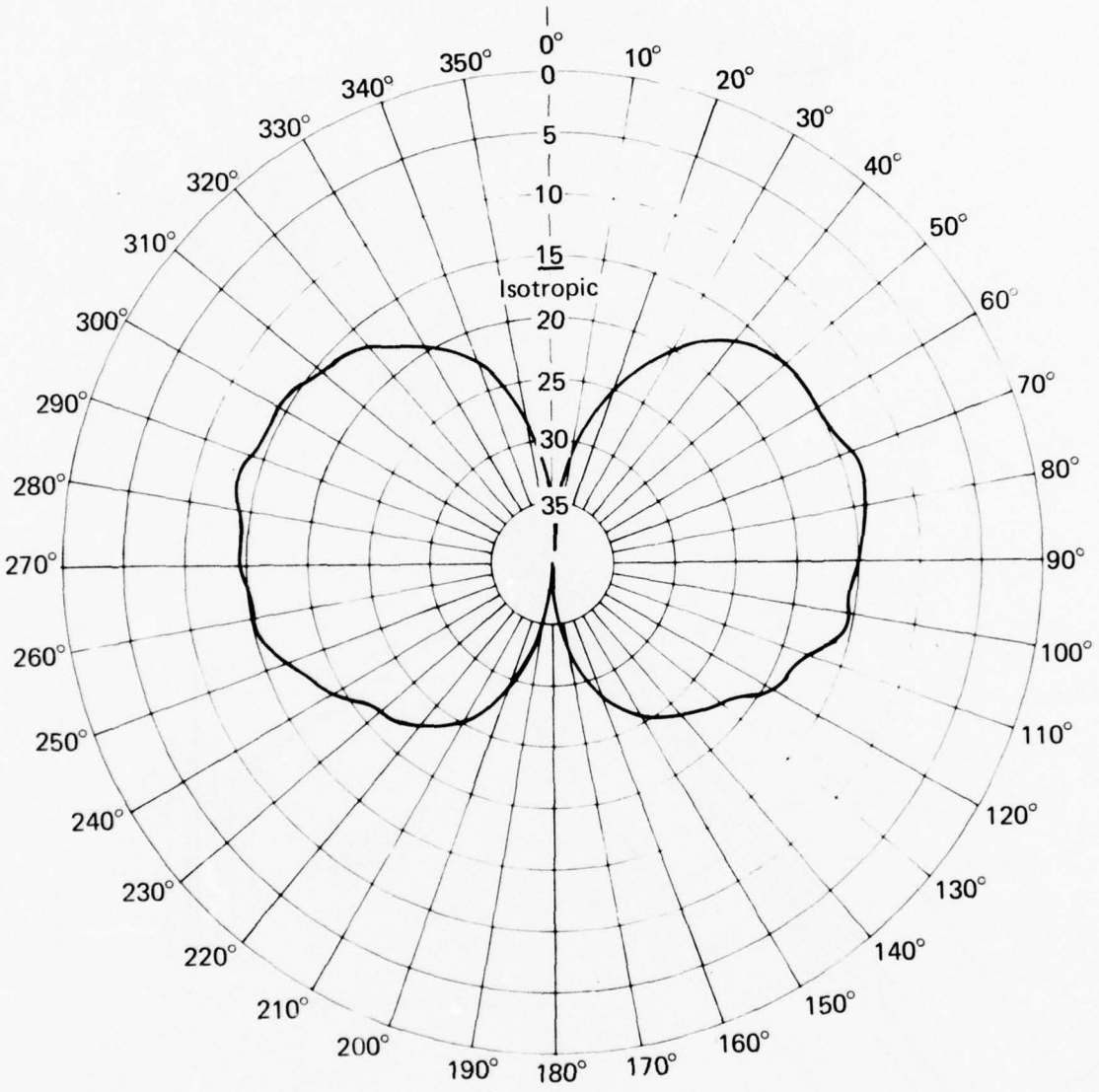


Fig. 7 Radiation Pattern of the 400-MHz Vertical Dipole

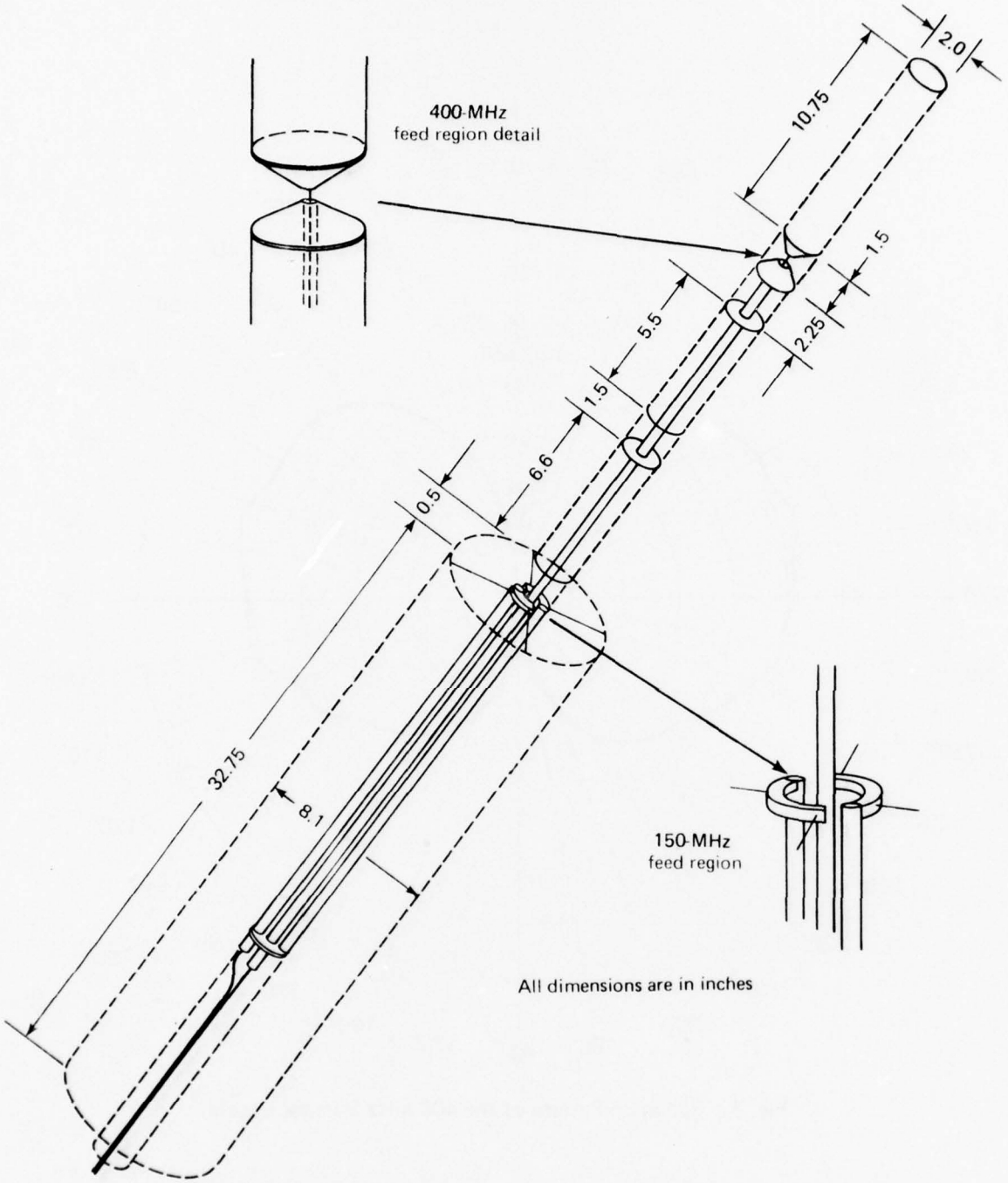


Fig. 8 Construction Detail of the NAVPAC Antenna

The 400-MHz coaxial feed continues inside the center tube to the feed region. The center conductor of the coaxial feed is connected to the upper feed cone and the lower cone is shorted to the coaxial shield and center tube. The two disks shown in the figure below the feed cones are also shorted to the center tube.

The quadrifilar helix is matched in its feed balun by the use of a $\lambda/4$ coaxial transformer. The matching of the dipole is also done by a coaxial transformer located in the center tube that feeds the dipole.

Mechanical Construction

The major mechanical problem in the antenna construction was that of providing good structural support over its full 61-in. length. The support is provided by a fiberglass center tube having a 2-in. diameter and a 1/16-in. wall. The tube spans the entire antenna length and houses the feed balun and cables. Support for each of the 150-MHz helix elements is derived from the center tube by four sets of struts. Each strut set consists of four 1/8-in. fiberglass tubes fastened to the center support tube by a collar.

The antenna elements are secured to the fiberglass tube after the feed structure is positioned inside it. The 400-MHz antenna elements are made from 0.003-in. shim brass formed into a tube and positioned over the fiberglass center tube. Each element is then connected to the feed cones and disks by eight screws. The 150-MHz antenna elements (0.1-in. diameter beryllium copper tubing) are soldered onto the balun extensions at the feed and are shorted to a ring at the base of the antenna.

RF PRESELECTORS AND PREAMPLIFIERS

The dual-channel NAVPAC receivers receive Doppler navigation signals at levels as low as -140 dBm. These low levels result in a design requirement that the front-end circuitry exhibit the lowest practical noise figures while also providing a high degree of selectivity to prevent interference from a multitude of unwanted signals. To accomplish these objectives, each of the two channels incorporates a two-stage RF preamplifier optimized for low noise figure. This preamplifier is preceded by a three-section bandpass filter exhibiting low loss and high selectivity. Together, these devices provide a system noise figure of about 2.3 dB at 150 MHz and 3.5 dB at 400 MHz.

Each of the two preselection filters is a 0.01-dB Chebishev design employing helical resonators. The basic electrical performance achieved with the filters is summarized in Table 3. The 150-MHz filters have TNC connectors and the 400-MHz filters have SMA connectors. This choice of connectors was made to prevent accidentally connecting a filter to the wrong antenna element.

Table 3

Typical Performance Summary of Preselection Filter

Parameter	Low Channel	High Channel
Center Frequency	150 MHz	400 MHz
Insertion loss	1.3 dB	1.3 dB
3-dB bandwidth	2.0 MHz	4.2 MHz
60-dB bandwidth	21.0 MHz	50.0 MHz
Stop-band rejection	>70 dB	>70 dB

Each preamplifier contains two cascaded common-emitter stages with input matching networks adjusted for minimum noise figure. Schematics for these amplifiers are shown in Figs. 9 and 10. Typical amplifier performance is summarized in Table 4.

Table 4

Summary of Preamplifier Performance

Parameter	Low Channel	High Channel
Center Frequency	150 MHz	400 MHz
Gain	29 dB	23 dB
Noise figure	1.0 dB	2.2 dB
3-dB bandwidth	30 MHz	40 MHz
1-dB compression	-7 dBm	+4 dBm
Gain margin	23 dB	16 dB

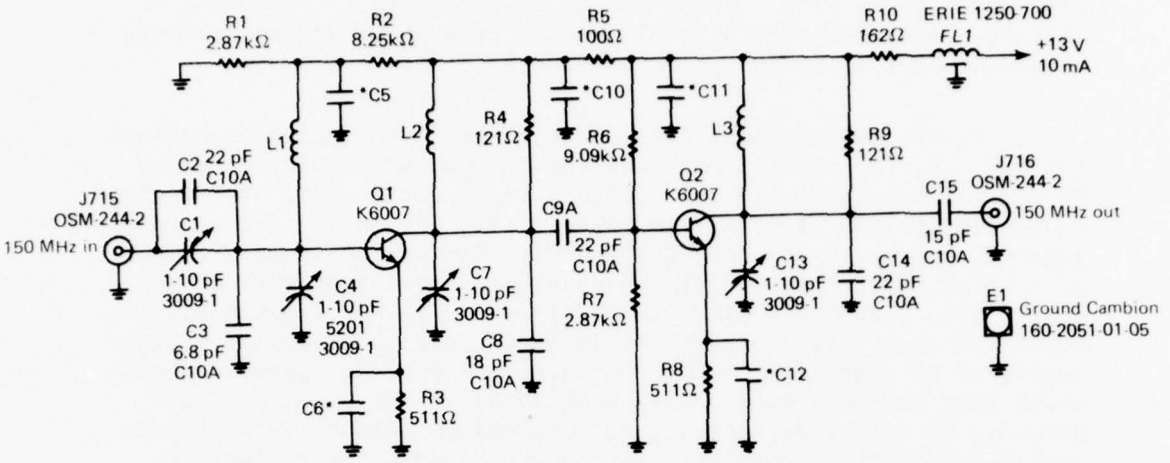


Fig. 9 Schematic Diagram of the 150-MHz Amplifier

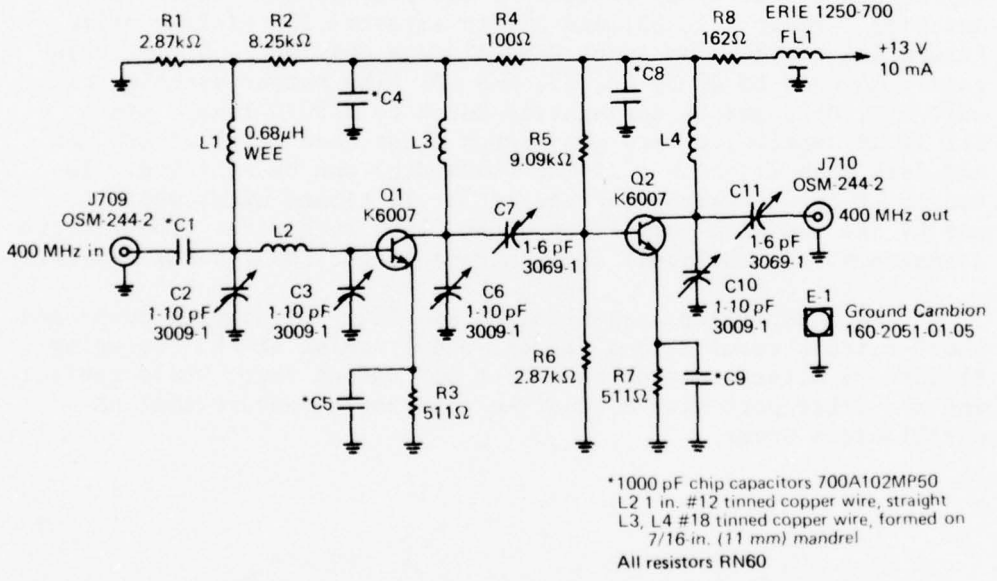


Fig. 10 Schematic Diagram of the 400-MHz Amplifier

The amplifiers are powered from the regulated +13-V bus and draw about 10 mA each. Power ground is connected to the metal chassis. The transistors are low-noise type K6007 devices and are biased at approximately V_{CE} = 10 V and I_E = 4 mA.

In the 150-MHz amplifier (Fig. 9) the input matching network (C1, C2, C3, C4, and L1) provides the optimum source impedance to Q1 for minimum noise figure. Since this is not a conjugate match, a high input VSWR results (less than 3:1). The interstage is conjugately matched by L2, C7, C8, and C9. The output is matched to 50 Ω by L3, C13, C14, and C15, providing a low output VSWR of typically less than 1.4:1 (less than 2:1 over a 15-MHz bandwidth). The 121-Ω shunt resistors in the collector circuits provide a high degree of RF stability, limit the gain, and provide increased bandwidth that reduces temperature sensitivity of the tuned circuits. However, R9 also reduces the 1-dB compression point. Chip capacitors are used throughout for RF bypasses because their leadless construction provides excellent low impedances at the operating frequencies. Inductors are air-wound solenoids made with No. 18 tinned wire. An EMI filter is included in the power bus. Components are mounted on an epoxy-glass PC board housed in a machined aluminum enclosure. Input and output connectors are SMA. Solder terminals are provided for power and ground connections.

The circuit configuration for the 400-MHz amplifier (Fig. 10) is nearly identical to that of the 150-MHz amplifier. Input matching circuit (C2, C3, and L2) is adjusted for minimum noise figure and provides an input VSWR of less than 3:1. Q1 is conjugately matched to Q2 by C6, C7, and L3. The output matching circuit C10, C11, and L4 conjugately match to a 50-Ω load. Since C11 is adjustable, a very good match (less than 1.1:1 at 400 MHz and less than 2:1 over a 15-MHz bandwidth) can be achieved. Inductor L2 is a straight section of No. 12 tinned wire, while L3 and L4 are one-half turn loops of No. 18 tinned wire. Construction, connectors, and enclosure are the same as for the 150-MHz amplifier.

Each amplifier is tested for stability by placing open- and short-circuit terminations (at all phase angles at the operating frequency) alternately at the input and output ports while monitoring the other port with a spectrum analyzer to ensure that no oscillations occur.

FIRST IF AMPLIFIERS

The first IF amplifiers (a portion of the NAVPAC RF section) perform more functions than just IF gain. The units contain the first mixers, and the output of each unit is split into three signals having equal power for driving the DTL's. Therefore, each has two inputs (RF and local oscillator) and three identical outputs with all ports specified to be 50 Ω. The overall net gain of each unit is specified to be 52 dB. The units are designed to have 1% bandpasses. In normal operation the maximum rms noise power out of either channel is approximately -37 dBm. The maximum signal level expected out of either unit is approximately -20 dBm. Each is designed to provide linear operation (i.e., power delivery capability) to these levels plus some margin; each exhibits a 1-dB compression point of about -10 dBm. A block diagram applicable to each is shown as Fig. 11.

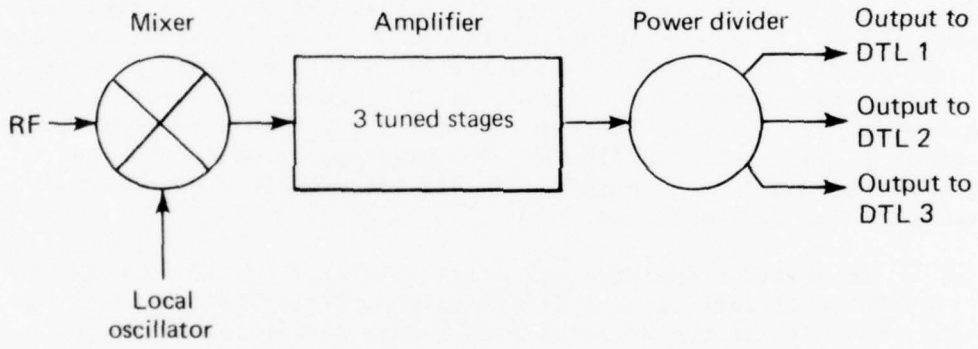


Fig. 11 Block Diagram of the First IF Amplifier

The mechanical design was made identical for both the high- and low-channel first IF so that only one layout and one set of chassis drawings would be required. The chassis construction is simple. The pieces required to make the multicompartment box are chemically milled out of 15-mil beryllium-copper. Copper corner posts (with machined-through holes and slots for seating the beryllium-copper walls) are assembled on a holding jig, and the chassis is soldered together using a hard solder. The chassis is then silver-plated and is ready to have the electronic components assembled into it.

The electrical design began with selection of a miniature double-balanced low-noise mixer. The conversion loss of the mixer is about 8 dB. A miniature three-way power divider (manufactured by the same company that made the double-balanced low-noise mixer) was chosen to provide the three equal outputs. The three-way power split results in a 4.8-dB loss. If an insertion loss of 1 dB to the power divider is assumed, then the total loss in the unit (rounded off to the nearest decibel) is 14 dB. The required amplifier gain is at least 66 dB when the overall net gain is specified to be 52 dB.

The design proceeded with the assumption that at the relatively low frequencies at which these IF's operate (i.e., 64 and 24 MHz) the required gain could be realized with three cascaded tuned amplifier stages. The 1% bandpass of the high channel is 640 kHz, and a simple calculation shows that the bandwidth of each stage of a cascaded three-stage tuned amplifier must be 1.25 MHz to provide the overall bandwidth of 640 kHz. Each of the tuned stages consists of a single-pole filter (simple tank circuit) that is assumed to be operating at an impedance level of 1 kΩ. Further calculations show that the required circuit values are 49 nH in parallel with 127 pF. The best approximation to 49 nH was provided by three turns of No. 20 copper wire on a 1/4-in. I.D. air core. A corresponding calculation for the low channel resulted in a single-stage bandwidth of 471 kHz. The required circuit values were found to be 130 nH in parallel with 338 pF. The best approximation to the 130 nH was found to be provided by six turns of No. 20 copper wire on a 1/4-in. I.D. air core.

The K2117 transistor was originally selected for use in the first IF amplifiers because it was being used in the second IF amplifiers (part of the dual-tracking loop), thereby reducing the number of different types of devices used in NAVPAC. However, it proved to be unstable in the first IF amplifiers and its use was abandoned. The 2N3339 was then used successfully in the low-channel unit, but it also proved to be unstable at 64 MHz. The 2N918, a lower gain device, was substituted into the high-channel unit and used successfully. Although all flight units were fabricated using 2N918 and 2N3339 devices as described, the 2N918 could be used in any future units if the 2N3339 devices should become unavailable.

Evaluation of the engineering models and test data from the six sets of flight units have shown that the design parameters have been realized within reasonable tolerances. Unbypassed emitter resistors were added to provide some degree of gain adjustment. This gain adjustment proved to be useful in the low-channel units;

however, all of the high-channel units have just met the gain specification with no negative feedback. A summary of the performance parameters is given in Table 5.

Table 5

Summary of First IF Amplifier Performance

Parameter	High Channel	Low Channel
RF frequency	400 MHz	150 MHz
LO frequency	336 MHz	126 MHz
LO input power	+6 dBm	+6 dBm
IF frequency	64 MHz	24 MHz
Overall net gain	52 dB	52 dB
3-dB bandwidth	640 kHz	240 kHz
Outputs	3 equal-power outputs	3 equal-power outputs
1-dB compressions (each output)	-10 dBm	-10 dBm
Impedance (all ports)	50 Ω	50 Ω
Power-supply voltage	-13 V	-13 V
Power-supply current	6.5 mA	6.5 mA

FREQUENCY SYNTHESIZER

The frequency synthesizer is defined as that portion of the NAVPAC electronics receiving its input signal from the 5-MHz ultrastable oscillator and supplying outputs that are reference frequencies coherent with the stable oscillator. The block diagram (Fig. 12) illustrates how the circuitry was partitioned to facilitate packaging and fabrication.

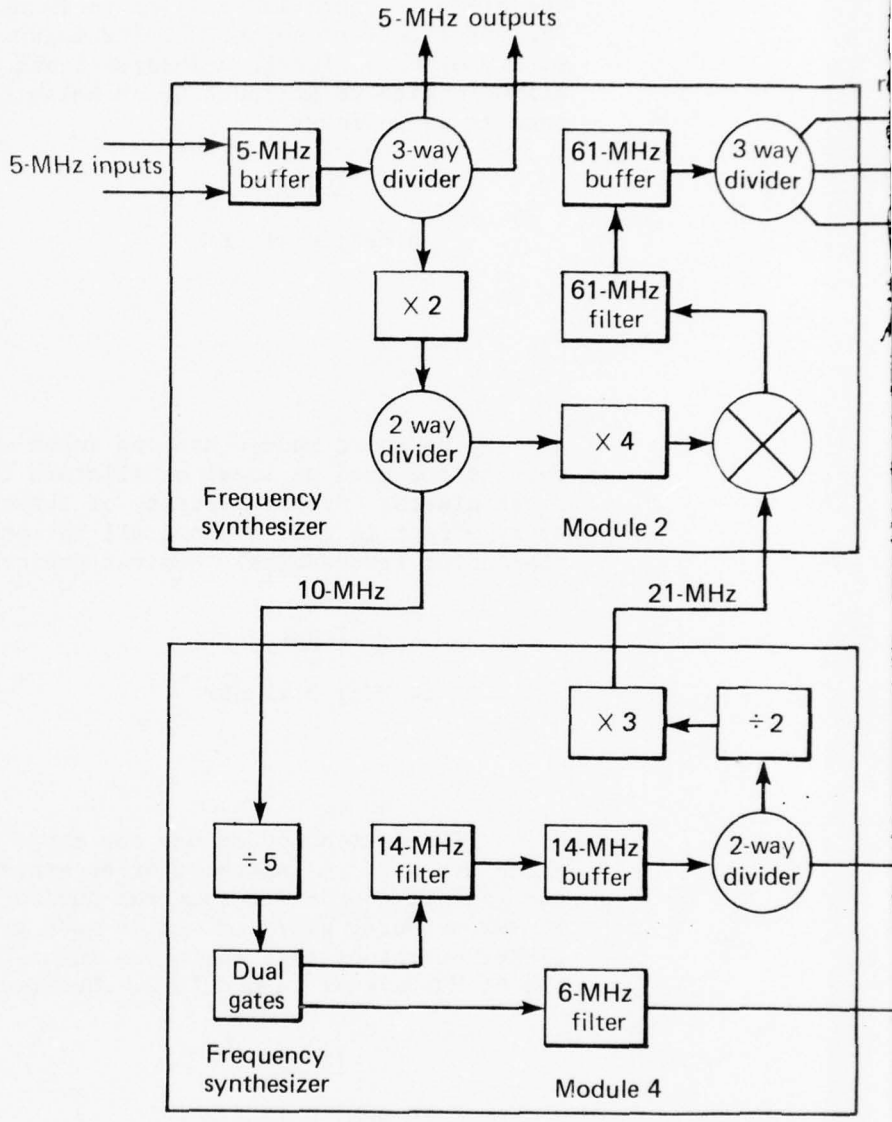
The synthesizer is divided into four major modules. This division balances the amount of electronics in each module and minimizes the number of module interconnections. The modules and their nomenclature are as follows:

Module	Nomenclature
1	12/18-MHz references
2	5/10-MHz buffers and 61-MHz references
3	126/336-MHz local oscillators
4	6/14/21-MHz generator

The first module has one input and six outputs. They are used in the DTL's as reference signals to the phase comparators and consequently do not have rigid requirements on their spectral purity. However, a design goal was chosen such that harmonics are about 40 dB below the center frequency. Desired performance is as follows:

Input	Outputs
6 MHz; -16 ±1 dBm	12 MHz; 0 ±1 dBm
	18 MHz; 0 ±1 dBm

The second module has three inputs: two from the 5-MHz stable oscillator and one 21-MHz input from the fourth module. It has six outputs: two buffered 5-MHz outputs, one 10-MHz output, and three identical 61-MHz outputs. One of the 5-MHz outputs is used as a clock source in the DPU while the other is a test monitor to be made available at the test-interface connector. The 10-MHz


5-MHz outputs
5-MHz inputs
5-MHz buffer
3-way divider
61-MHz buffer
3 way divider
X 2
61-MHz filter
2 way divider
X 4
Frequency synthesizer
Module 2
10-MHz
21-MHz
X 3
÷ 2
÷ 5
14-MHz filter
14-MHz buffer
2-way divider
Dual gates
6-MHz filter
Frequency synthesizer
Module 4

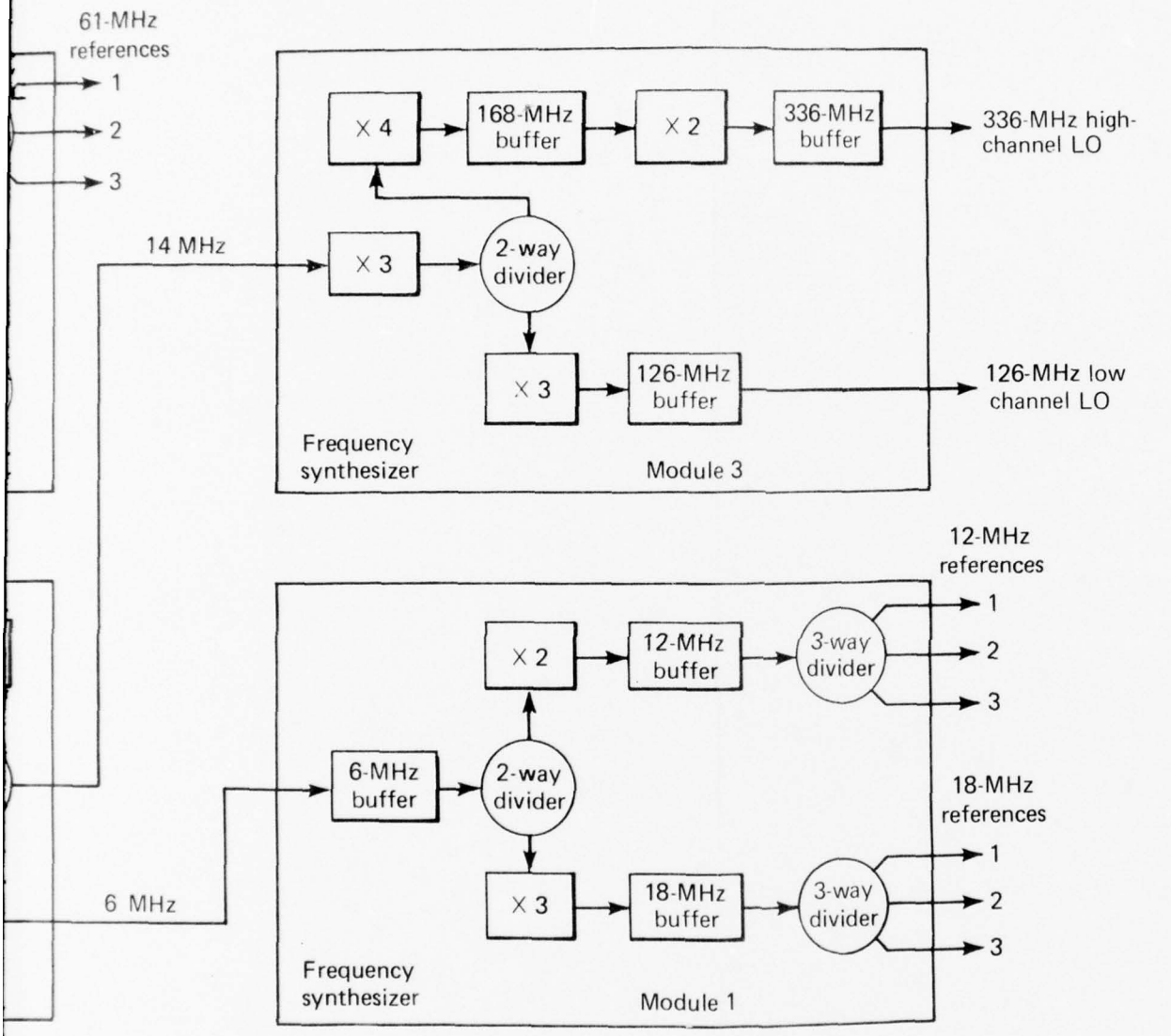


Fig. 12 Block Diagram of the Frequency Synthesizer

output is used as an input to another synthesizer module. The goals for spectral purity stated for module 1 also apply to these outputs. The 61-MHz outputs are used as an input to a mixer in each of the DTL's for converting the Doppler measurement to baseband. Spectral purity of this signal is important and every effort is made to hold all harmonics to at least 40 dB below the 61 MHz. Desired performance is as follows:

Input	Outputs
5 MHz; 0 ±1 dBm	5 MHz; 0 ±1 dBm
	10 MHz; 0 ±1 dBm
	61 MHz; -3 ±1 dBm

The third module has one input and two outputs. The two outputs are used as local oscillators to the high- and low-channel first mixers. Spectral purity of these signals is critical and every effort is made to hold all harmonics to at least 40 dB below the center frequencies. Desired performance is as follows:

Input	Outputs
14 MHz; 3 ±1 dBm	126 MHz; 6 ±1 dBm
	336 MHz; 6 ±1 dBm

The fourth module has one input and three outputs, all of which are used as inputs to other synthesizer modules. Whereas the goal of -40 dB for spectral purity is applied to the 6- and 14-MHz outputs, every effort is made to obtain this purity on the 21-MHz output because it is one input to a mixer used to generate the 61-MHz signal in module 2. Desired performance is as follows:

Input	Outputs
10 MHz; 0 ±1 dBm	6 MHz; -16 ±1 dBm
	14 MHz; 3 ±1 dBm
	21 MHz; 6 ±1 dBm

Total power consumption for the four synthesizer modules is 710 mW.

REFERENCE OSCILLATOR

Design

The oscillator package consists of two independent oscillators in a single enclosure. Only one of the oscillators can be operated at any given time. The package occupies 58 in^3, weighs 2.4 lb, and typically requires 0.63 W from a DC power source at an ambient temperature of 25°C and at a pressure of 10^{-5} Torr. Figure 13 is a block diagram of one of the independent oscillators. The oscillator stage is a modified Pierce circuit in which negative feedback is used to reduce flicker noise and stabilize circuit gain.

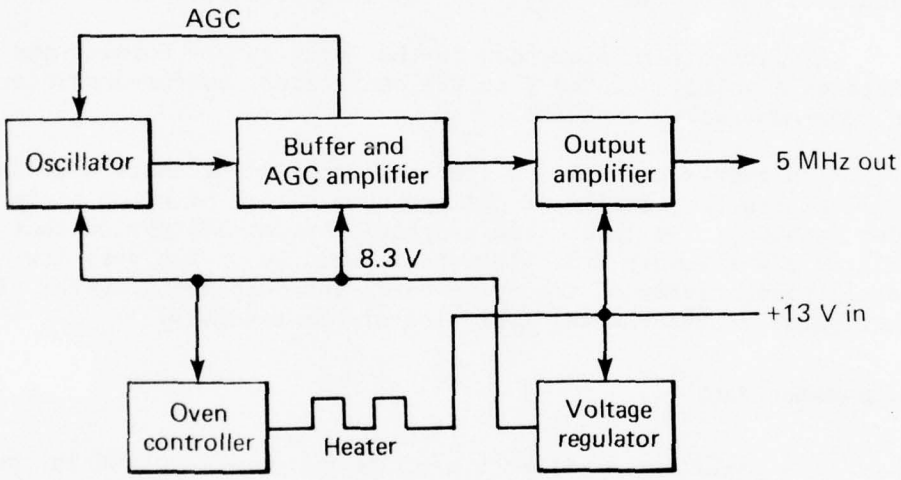


Fig. 13 Block Diagram of the 5-MHz Quartz Oscillator

A 5-MHz fifth overtone quartz crystal is the frequency control element. A buffer and AGC amplifier follow the oscillator stage, increasing the 5-MHz signal level and developing an AGC voltage. The AGC voltage is applied to the oscillator stage to maintain a constant-level drive to the quartz crystal.

The buffer is followed by an output amplifier that increases the 5-MHz power level to drive an external load and provide isolation from external load variations.

The oven controller includes a thermistor in one leg of a resistive balanced bridge to sense temperature changes. The error signal from the bridge is amplified and used to control power to a heater that maintains the turning point temperature of the quartz crystal to within 0.001°C. Both the oscillator stage and the oven controller are implemented using hybrid-circuit fabrication techniques to minimize volume within the temperature controlled area.

A "super insulation," consisting of alternate layers of radiation-reflective aluminized Mylar and a porous low-thermal conductivity Tissuglas paper, is used in the oscillator package. This form of insulation has a thermal conductivity that is three orders of magnitude less than urethane foam. In order to realize the insulating qualities of super insulation, the system must be evacuated to a pressure of 10^{-4} torr, accomplished simply by venting the enclosure to the vacuum of outer space, once orbit has been achieved.

A voltage regulator reduces the input supply voltage and maintains a voltage of 8.3 V to the oscillator, buffer-amplifier, and oven-controller circuits.

The quartz crystal and its supporting electronics are suspended within the oscillator package by a series of nylon cords under tension. The cords form a dynamic suspension system that isolates the assembly from vibration. Because of the very low thermal conductivity of the nylon cord, the suspension system also contributes to the thermal isolation of the assembly.

Performance Data

The goals for oscillator performance were realized in the present design. Figure 14 shows typical 24-h drift rates for two oscillators. Data for oscillator A cover a 14-day period and have an average daily drift rate of 1.58×10^{-11}. Oscillator B has an average daily drift rate of 1.94×10^{-11} for a 17-day period. A plot of fractional frequency stability (Allan variance) for averaging times (τ) from 0.1 s to 1000 s is presented in Fig. 15 (measurement system noise bandwidth is 60 kHz). Figure 15 is a composite of data from several oscillators; the bar at each τ indicates the maximum and minimum data from the group of oscillators. The line connecting the various averaging times is the average Allan variance for the group of oscillators.

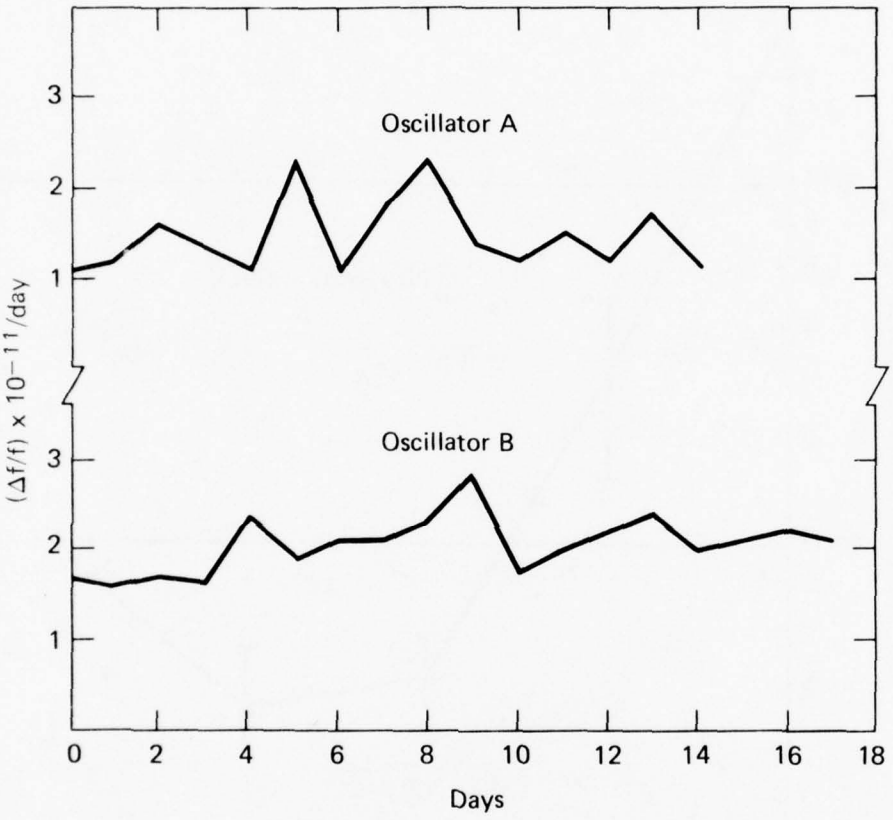


Fig. 14 Typical 24-Hour Drift Rate for Two Oscillators

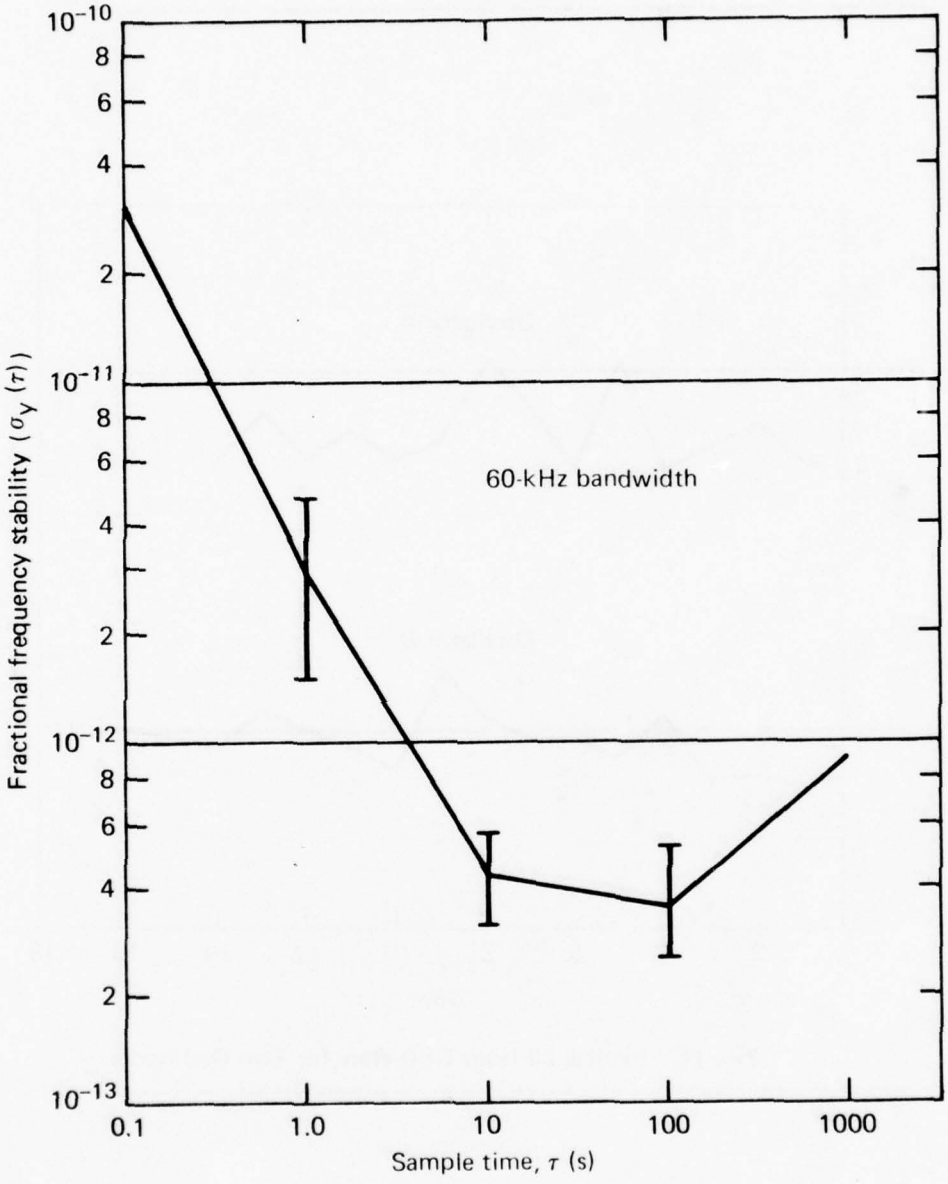


Fig. 15 Allan Variance versus Sample Time

Other operating parameters are:

1. Frequency shift resulting from a change in input power supply voltage of ±5% is 6.42×10^{-12}/V.

2. Spurious response

   Harmonic: 55 dB below 5-MHz carrier

   Nonharmonic: 65 dB below 5-MHz carrier in 100 Hz bandwidth

DUAL TRACKING LOOPS (DTL)

400-MHz Reception

The upper right corner of Fig. 5 illustrates the 400-MHz or high channel of the DTL. The input signal to the high channel is one of the outputs from the high channel first IF.

$$\text{High channel input} = 64\ \text{MHz} + f_H + d_H + e_H,^*$$

where

$f_H \equiv$ -80 ppm offset referred to 400 MHz,

$d_H \equiv$ Doppler shift at 400 MHz, and

$e_H \equiv$ refraction error at 400 MHz.

The input signal passes through a voltage controlled attenuator (VCA) that is used to maintain a constant level in the phase-locked loop. The output of the VCA is mixed with a signal from the second LO synthesizer such that

$$\text{Second IF frequency} = \underbrace{(64\ \text{MHz} + f_H + d_H + e_H)}_{\text{First IF output}} - \underbrace{(61\ \text{MHz} + f_H + d_H + e_H)}_{\text{Second LO synthesizer}}$$

$$= 3\ \text{MHz}.$$

* The 64 MHz first-IF frequency is derived by mixing the received 400 MHz + $f_H + d_H + e_H$ signal with a 336-MHz reference signal in the first mixer.

The 3-MHz signal is then amplified by the second IF amplifier (a three-stage amplifier containing a single-pole crystal filter having a two-sided 3-dB bandwidth that is approximately 1.2 kHz). The second IF output is divided in a three-way power splitter for:

1. The stop-sweep detector, used for automatic acquisition;

2. The main phase detector, used to phase lock the loop and to derive the sine portion of the NAVSAT modulation; and

3. The auxiliary phase detector, used for coherent AGC (automatic gain control) and to derive the cosine portion of the NAVSAT modulation.

The stop-sweep detector consists of a single-pole crystal filter with a two-sided 3-dB bandwidth of about 60 Hz, a diode detector, and a comparator. During acquisition, the signal level out of the diode detector is compared to a fixed preset level when a signal in the IF amplifier is within the passband of the stop-sweep crystal filter. The output of the comparator changes the high-channel phase locked loop (HCPLL) from an open-loop sweep mode to a closed-loop track mode.

The output of the main phase detector is a function of the amplitude of its input signal and the phase difference between the input and a 3-MHz reference signal (derived from the frequency synthesizer). The phase-error signal, after it has been amplified and filtered by the loop filter, is applied to the 30.484-MHz voltage-controlled crystal oscillator (VCXO). The frequency of the VCXO output is doubled in the second LO synthesizer and becomes the local-oscillator reference frequency in the high-channel second mixer at the input to the high-channel second IF amplifier, closing the high-channel phase-locked loop.

The inputs to the auxiliary phase detector are the signal from the IF amplifier and a 3-MHz reference signal that is shifted in phase by 90° relative to the 3-MHz signal used for the main phase detector reference. The output of the auxiliary detector is a signal having a DC component that represents the rms value of the signal in the IF amplifier. This signal is low-pass filtered by the AGC amplifier and is used to drive the VCA for coherent AGC. The result is a constant preset signal level in the IF amplifier. Because of the closed-loop AGC system, the phase detector outputs are not affected by varying RF signal levels until the RF signal decreases out of AGC control range.

The VCA is a π-section diode network, having the design characteristic of virtually no phase-shift variations as a function of signal level. The AGC amplifier characteristics are shaped in an attempt to make the net function of the VCA linear in terms of dB/V control. The result is an AGC system having a time constant that is relatively constant at all signal levels (see Appendix B).

The "reconstructed high-channel Doppler" signal is obtained by mixing the high-channel output of the second LO synthesizer with a 61-MHz reference signal from the frequency synthesizer. The result is a Doppler frequency represented by

$$61\ \text{MHz} - (61\ \text{MHz} + f_H + d_H + e_H) = -(f_H + d_H + e_H).$$

Example:

Assume $d_H = +10$ kHz,

$e_H = -2$ Hz, and

$f_H = -80\ \text{ppm} \times 400 = -32$ kHz.

Then the high-channel Doppler frequency equals

$$-(-32\ \text{kHz} + 10\ \text{kHz} - 2\ \text{Hz}) = 21.998\ \text{kHz}.$$

The high-channel Doppler signal contains refraction information and is therefore referred to as being "uncorrected" Doppler (as opposed to vacuum-corrected Doppler, which contains no refraction).

The 400-MHz NAVSAT signal is phase modulated by navigation-message and timing signals. The closed-loop bandwidth of the HCPLL is such that only the average phase of the RF signal (i.e., the carrier) is tracked. When a NAVSAT signal is being tracked, the average value of the main phase-detector output is near zero and the average value of the auxiliary phase-detector output represents the level of the carrier being tracked. The sine and cosine components of the phase modulation are also present at the outputs of the main and auxiliary phase detectors. The sine component (or doublet) is detected by the main phase detector, and the cosine component (doublet clock) is detected by the auxiliary phase detector. These signals are amplified and used to recover NAVSAT timing and identification information.

150-MHz Reception

The lower right corner of Fig. 5 illustrates the 150-MHz or low channel of the DTL. The input signal to the low channel is one of the outputs from the low channel first IF.

$$\text{Low channel input} = 24\ \text{MHz} + f_L + d_L + e_L,^*$$

where

$f_L \equiv$ -80 ppm offset referred to 150 MHz,

$d_L \equiv$ Doppler shift at 150 MHz, and

$e_L \equiv$ refraction error at 150 MHz.

The input signal passes through a VCA. The output of the VCA is mixed with a signal from the second LO synthesizer such that

$$\underset{\text{IF signal}}{\text{Second}} = \underbrace{(24\ \text{MHz} + f_L + e_L)}_{\text{First IF output}} - \underbrace{(22.875\ \text{MHz} + f_L + d_L + \tfrac{3}{8}e_H)}_{\text{Second LO synthesizer}^{**}}$$

$$= 1.125\ \text{MHz} + e_L - \tfrac{3}{8}e_H$$

---

* The 24-MHz first IF frequency is derived by mixing the received 150 MHz + $f_L + d_L + e_L$ signal with a 126-MHz reference signal in the first mixer.

** The second LO synthesizer signal is derived as follows: The high channel VCXO signal is doubled to close the HCPLL. This implies that

$$\text{VCXO signal} = \tfrac{1}{2} \times (61\ \text{MHz} + f_H + d_H + e_H)$$

$$= 30.5\ \text{MHz} + \frac{f_H + d_H + e_H}{2}\ .$$

(Note continues on next page.)

Observe that the second IF signal consists of a constant frequency plus terms related only to the high-channel and low-channel refraction errors. This configuration is often referred to as a "master/slave" receiver because the low channel (or slave) requires the master high channel to remove the low channel Doppler and offset parameters.

The output of the second mixer is amplified by the second IF amplifier, a three-stage amplifier containing a single-pole crystal filter whose two-sided 3-dB bandwidth is approximately 300 Hz. The output of this amplifier is divided in a two-way power splitter for:

1. The main phase detector, used for the low-channel phase locked loop (LCPLL); and

2. The auxiliary phase detector, used for coherent AGC and for automatic acquisition.

The second LO synthesizer also multiplies the VCXO signal by 3/4 to obtain

$$\text{Second LO signal} = 22.875\ \text{MHz} + \frac{3}{8}f_H + \frac{3}{8}d_H + \frac{3}{8}e_H.$$

The high-channel and low-channel Doppler and offset terms are related as:

$$f_L = \left(\frac{150}{400}\right) f_H = \frac{3}{8}f_H, \text{ and}$$

$$d_L = \left(\frac{150}{400}\right) d_H = \frac{3}{8}d_H .$$

Using these relationships, the second LO signal can be rewritten as

$$\text{Second LO signal} = 22.875\ \text{MHz} + f_L + d_L + \frac{3}{8}e_H .$$

The output of the main phase detector is a function of the amplitude of its input signal and the phase difference between the input and a reference signal (derived from a divide-by-4 network driven by the low channel VCXO). The phase-error signal, after it has been amplified and filtered by the loop filter, is applied to the low channel VCXO. Because the input and the reference to the main phase detector must be the same frequency to close the LCPLL, and because the VCXO frequency is divided by 4 prior to closing the loop, it follows that:

$$\text{VCXO frequency} = 4[1.125\ \text{MHz} + (e_L - \tfrac{3}{8}e_H)]^*$$

$$= 4.5\ \text{MHz} + 4(e_L - \tfrac{3}{8}e_H).$$

The VCXO frequency is also mixed with two 4.5-MHz signals (derived from the frequency synthesizer) that are separated in phase by 90° to derive refraction data. The net result of this operation is two $4(e_L - \frac{3}{8}e_H)$ signals, separated in phase by 90°. By combining these two signals in an up-down counter, it is possible to determine whether the refraction term is a positive or negative frequency.

The inputs to the auxiliary phase detector are the signal from the IF amplifier and the VCXO frequency divided by 4 and shifted 90° in phase (relative to the reference used in the main phase detector). This output signal is used to drive a closed-loop AGC system identical to that used in the HCPLL.

The output of this phase detector is also low-pass filtered (noise equivalent bandwidth = 20 Hz) at the input to the stop-sweep detector. If the output of the low-pass filter exceeds a preset positive or negative value during the acquisition phase, the stop-sweep level detector will change the LCPLL from an open-loop sweep mode to a closed-loop track mode.

High-Channel Phase-Locked Loop

An early examination of typical curves of the Doppler shift (that the NAVPAC DTL would have to receive) revealed two major items:

---

* e_L and e_H terms can have positive or negative signs.

1. The total 400-MHz Doppler shift could be as large as 40 kHz (±20 kHz about the nominal closest approach frequency of 399.968 MHz), and

2. The maximum 400-MHz Doppler rate-of-change that would be observed could be as high as 400 Hz/s.

Both of these parameters represent requirements that exceed those placed on most previous NAVSAT receiver sets. The ±20-kHz Doppler shift did not present any problems, but the 400 Hz/s rate term implied that if the phase-locked loop was only a second-order system (two integrators in the loop), the rate term would require the bandwidth to be extremely wide to limit the dynamic phase error. An alternative to a wide-bandwidth second-order system is a third-order loop (three integrators). This approach also has pitfalls in that third-order loops can introduce stability problems during acquisition. The configuration used in NAVPAC is sometimes referred to as a "two-and-one-half-order" loop in which a lossy integrator is added to a second-order loop, reducing the dynamic phase error but not introducing the instability problems of the third-order loop. The lossy integrator is a passive lag network (Fig. 16).

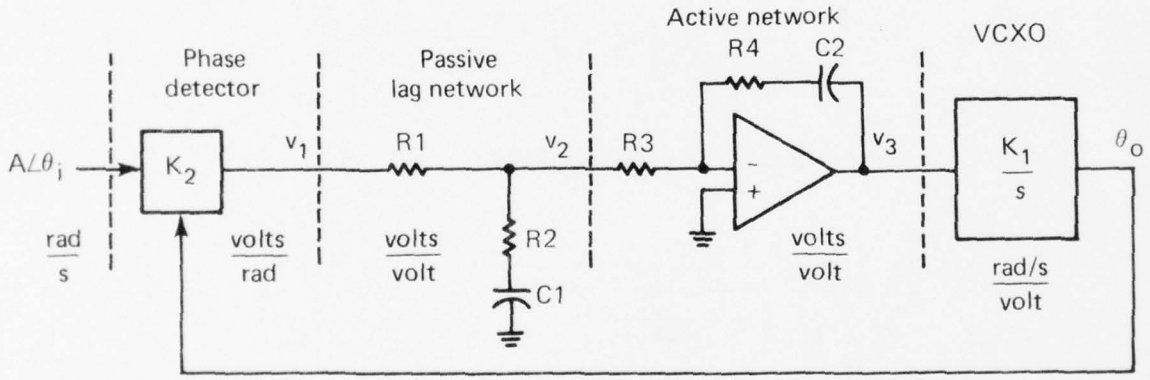


Fig. 16 The "Two-and-One-Half-Order" Loop (lossy integrator)

Figure 16 represents the basic phase-locked loop used in the DTL. An examination of Fig. 5 shows that the LCPLL is configured like Fig. 16, while the HCPLL has a slight variation at the point where the loop is closed and in what is used as reference for the phase detector. A closer look at Fig. 5 reveals that the HCPLL is still basically identical to Fig. 16. The phase-locked loop operates as follows:

1. The DTL phase detector is a double-balanced mixer having an output that is a voltage related to the amplitude of the $A\angle\theta_i$ input and the phase error $= \theta_i - \theta_o$, and is

$$\frac{\text{volts}}{\text{radian}} = 0.201\ 10^{\left(\frac{\text{dBm input}}{20}\right)} \quad \text{(see Appendix A)},$$

where "dBm input" is the power level of the input signal minus 1 dB (a practical value for insertion loss). The AGC in the DTL sets the level to -10 dBm, so that

$$K_2 = 0.201\left(10^{(10-1)/20}\right) \approx 57 \text{ mV/rad.}$$

2. The loop filter consists of the passive lag network and the active network. The transfer function of the passive network (v_2/v_1) is

$$\frac{v_2}{v_1} = \frac{s + \frac{1}{R_2C_1}}{\frac{R_1 + R_3}{R_2R_3}\left[s\left(R_2 + \frac{R_1R_3}{R_1 + R_3}\right) + \frac{1}{C_1}\right]}$$

This equation can be rewritten

$$\frac{v_2}{v_1} = \frac{s + \frac{1}{R_2C_1}}{\alpha_1'\left(s + \frac{1}{\alpha_1 R_2 C_1}\right)},$$

where

$$\alpha_1 \equiv \frac{R_2 + \frac{R_1R_3}{R_1 + R_3}}{R_2}$$

and

$$\alpha_1' \equiv \frac{R_1 + R_2}{R_2} + \frac{R_1}{R_3} \quad .$$

The transfer function of the active network is

$$\frac{v_3}{v_1} = \frac{R_4}{R_3} \left(\frac{s + \frac{1}{R_4 C_2}}{s} \right).$$

The DTL loop filter transfer function is now

$$\frac{v_3}{v_1} = \frac{R_4}{R_3} \left(\frac{\left(s + \frac{1}{R_2 C_1}\right)\left(s + \frac{1}{R_4 C_2}\right)}{s\left(s + \frac{1}{\alpha_1 R_2 C_1}\right)} \right) \frac{1}{\alpha_1'} \quad .$$

3. The frequency of the VCXO is determined by the input voltage v_3. Changes in frequency are determined by $\Delta\omega = K_1 v_3$ where K_1 is the VCXO gain constant in (radians/second)/volt. Because frequency is the derivative of phase, the VCXO output can be written as

$$\frac{d\theta_o}{dt} = K_1 v_3.$$

By transferring $\frac{d\theta_o}{dt}$ from the t-domain to the s-domain, the relationship can be rewritten

$$\theta_o = v_3(s) \left(\frac{K_1}{s}\right)$$

or, in other words, the phase of the VCXO output is the integral of input voltage. The VCXO now represents an integrator in the loop. The K_1 term must include any

multiplication or division involved with the VCXO output (e.g., if the VCXO has a $k_1 = 6.9 \times 10^3$ (rad/s)/V and is followed by a X2 multiplier, the K_1 term for the loop becomes $K_1 = 2k_1 = 13.8 \times 10^3$ (rad/s/V).

4. The overall open-loop function is then

$$\frac{\theta_o}{v_1} = K_2 \left[\frac{R_4}{R_3} \left(\frac{\left(s + \frac{1}{R_2C_1}\right)\left(s + \frac{1}{R_4C_2}\right)}{s\left(s + \frac{1}{\alpha_1 R_2 C_1}\right)} \right) \frac{1}{\alpha_1'} \right] \frac{K_1}{s}$$

For a critically damped system (damping coefficient = 1), this expression can be simplified using

$$\frac{\omega_o}{3} = \frac{1}{R_2C_1} = \frac{1}{R_4C_2}$$

and

$$\alpha_2 \equiv \frac{R_3}{R_4} ,$$

where

$B_L = 0.743\ \omega_o \equiv$ single-sided loop noise-equivalent bandwidth in Hz.

Therefore,

$$\frac{\theta_o}{v_1} = \frac{K_1 K_2}{\alpha_2 \alpha_1'} \left(\frac{\left(s + \frac{\omega_o}{3}\right)^2}{s + \frac{\omega_o}{3\alpha_1}} \right) \frac{1}{s^2} .$$

The procedure to set loop gain correctly requires

$$\frac{K_1 K_2}{\alpha_2 \alpha_1'} = \frac{9}{4}\omega_o \ .$$

Before loop parameters can be selected, the acceleration-error coefficient ($\mathcal{E}$) representing the Doppler rate term must be considered. Because the passive lag network is not a true integrator, the rate error term is not zero (although it is reduced by a 2½-order loop when compared to a second-order loop). The steady-state acceleration error coefficient for the DTL is

$$\mathcal{E}_{ss} = \frac{4.619\ \dot{d}}{\alpha_1\ B_L{}^2} \text{ rad},$$

where

$\dot{d}$ = maximum Doppler rate of change (in Hz/s) to be tracked.

$\mathcal{E}_{ss}$ should not exceed about 0.1 rad if the term is not to become a major source of error in the system. The α_1 term* (a function of the passive lag-network resistors and the input resistor to the active network) can be thought of as the improvement factor to $\mathcal{E}_{ss}$ that is due to the lag network.

---

* The α_1 term can be simplified by setting $R_1 = R_3$. A good starting value for α_1 is about 20. While these choices seem arbitrary, it can be shown that they result in about the lowest R_1, R_3, and C_2 values. Because of value spacings of resistors and capacitors, it may be necessary to vary these parameters slightly.

The HCPLL parameters chosen were

$$\varepsilon_{ss} = 0.1 \text{ rad}$$

for

$$\dot{d} = 400 \text{ Hz/s},$$

$$\alpha_1 \approx 20,$$

$$B_L = 30 \text{ Hz},$$

and

$$\omega_o = 40.38 \text{ rad/s}.$$

The loop filter components can then be calculated with values for K_1 and K_2 from the discussion of the VCXO and phase detector.

Low-Channel Phase-Locked Loop

The LCPLL must acquire and track the difference-frequency term, which is related to the refraction error. This term, $e_L - \frac{3}{8}e_H$, has been estimated to be limited to ≤ 150 Hz with peak rates ≤ 50 Hz/s. The LCPLL has the same 2½-order characteristics as the HCPLL, but the loop parameters are different. The requirements of the LCPLL were not well defined during the early design phase; therefore, parameters were originally selected that turned out to be less than optimum and were difficult (if not impossible) to change later.

1. The phase detector constant (K_2 of Fig. 16) is set at $K_2 = 57$ mV/rad as in the HCPLL.

2. The total VCXO gain constant was set at $K_1 = 30\pi$ (rad/s)/V (i.e., 15 Hz/V). This K_1 includes the ÷4 term required to close the loop. The k_1 scaling directly at the VCXO output is therefore 60 Hz/V. With a maximum input of ±10V at the input to the VCXO, the

variation of ±600 Hz at the VCXO output (refer to Fig. 5) represents the maximum frequency corresponding to the refraction data.*

The effect of some early parameter choices for the LCPLL resulted in final parameters of $\alpha_1 = 5.2$ and $\alpha_2 = 0.0075$ for $B_L = 20$ Hz. (These are hardly ideal values, but they illustrate how early design decisions can affect the final configuration.)

Receiver Controller

Each DTL contains an electronics board called the Receiver Control. This board contains the search, acquisition, and track-control electronics for the high- and low-channel phase-locked loops, as well as some peripheral circuits such as a telemetry interface to allow in-orbit monitoring of the status of the loops (i.e., in search or track modes, locked or unlocked). Figures 17 and 18 are logic flow charts illustrating the receiver-control processes.

Low-Channel Controller. The low-channel control logic is relatively simple. With the loop open, a search pattern is generated by a triangular sweep that has a maximum frequency of ±150 Hz. The + to - to + period of this pattern is 12 s, which corresponds to a search rate of 50 Hz/s. The search frequency, which is the reference to the phase detectors, effectively scans the output of the second IF amplifier until an output from the stop-sweep detector stops the sweep and closes the loop. If the loop locks to the signal before an internal timer overflows, the loop is considered locked and the DPU is informed that differential-Doppler or refraction data are available. If the loop does not lock to the signal before the timer overflows, the loop is opened and the search

---

* To a first-order approximation, the refraction error is inversely proportional to the transmitted frequency. The low-frequency term e_L can therefore be approximated as $e_L = \frac{8}{3}e_H$; hence the refraction term at the output of the VCXO can be written

$$4(e_L - \frac{3}{8}e_H) = 4(\frac{8}{3}e_H - \frac{3}{8}e_H) = 9\frac{1}{6}e_H.$$

In other words, the refraction information from the DTL is a frequency that is about $9\frac{1}{6}$ times the refraction error at 400 MHz.

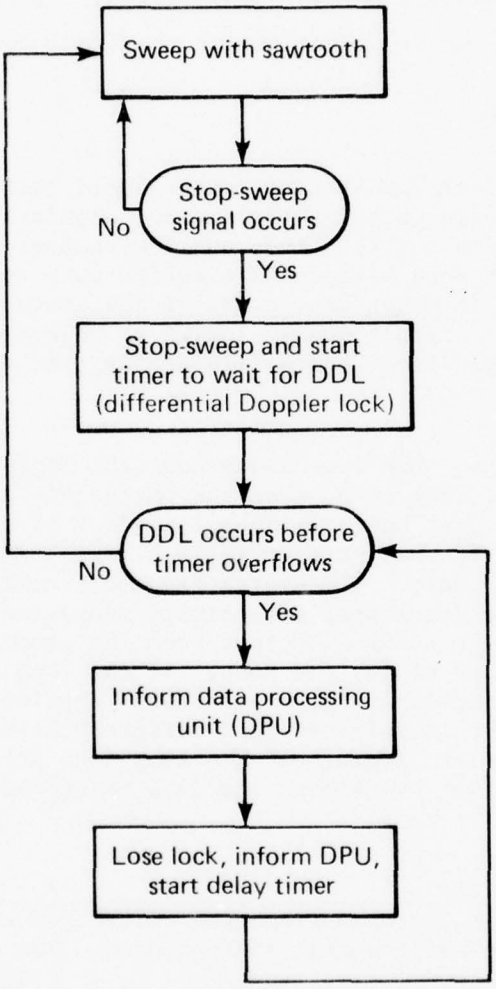
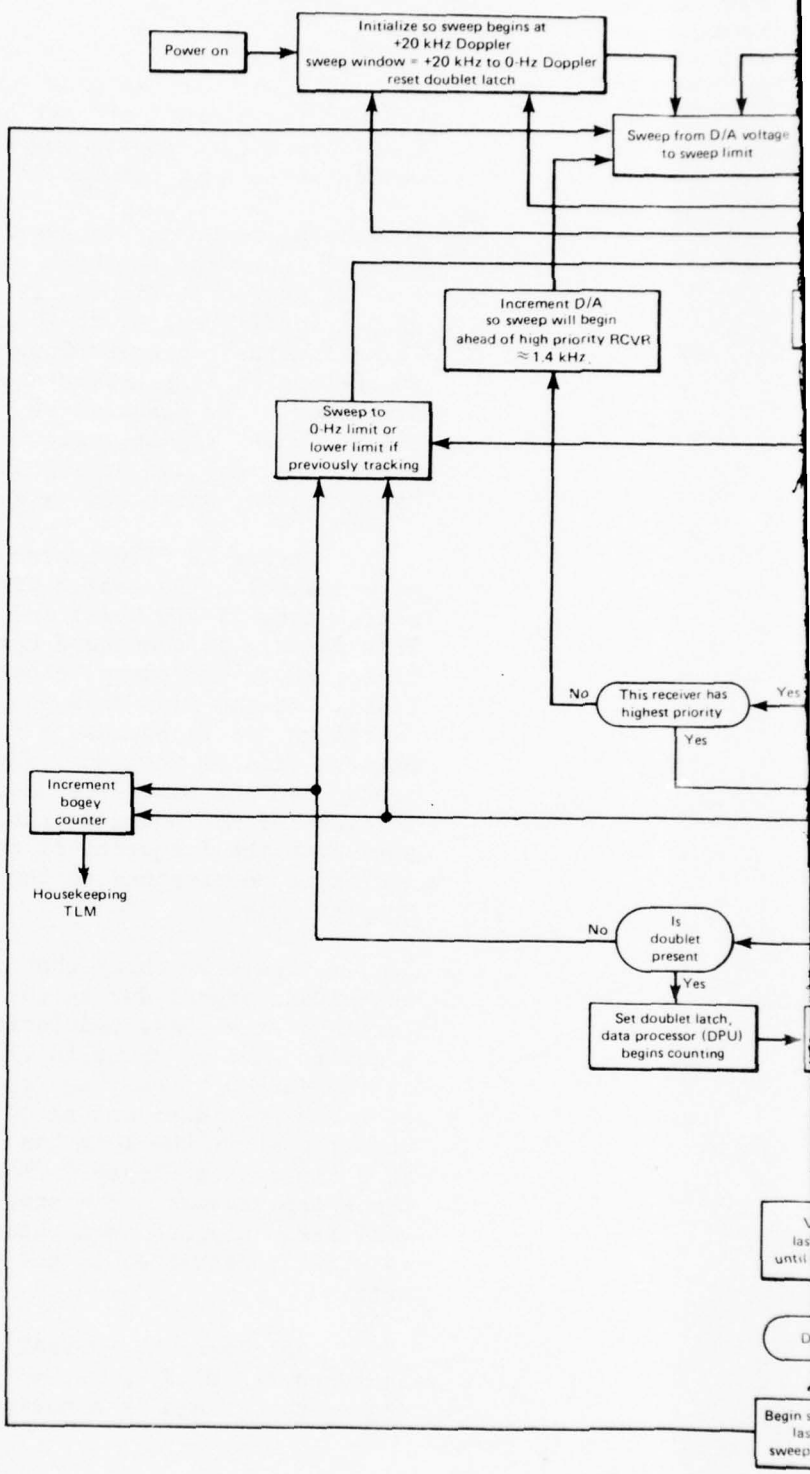


Fig. 17 Flow Diagram for 150-MHz Acquisition


Power on
Initialize so sweep begins at
+20 kHz Doppler
sweep window = +20 kHz to 0-Hz Doppler
reset doublet latch
Sweep from D/A voltage
to sweep limit
Increment D/A
so sweep will begin
ahead of high priority RCVR
≈1.4 kHz
Sweep to
0-Hz limit or
lower limit if
previously tracking
No
This receiver has
highest priority
Yes
Yes
Increment
bogey
counter
Housekeeping
TLM
No
Is
doublet
present
Yes
Set doublet latch,
data processor (DPU)
begins counting

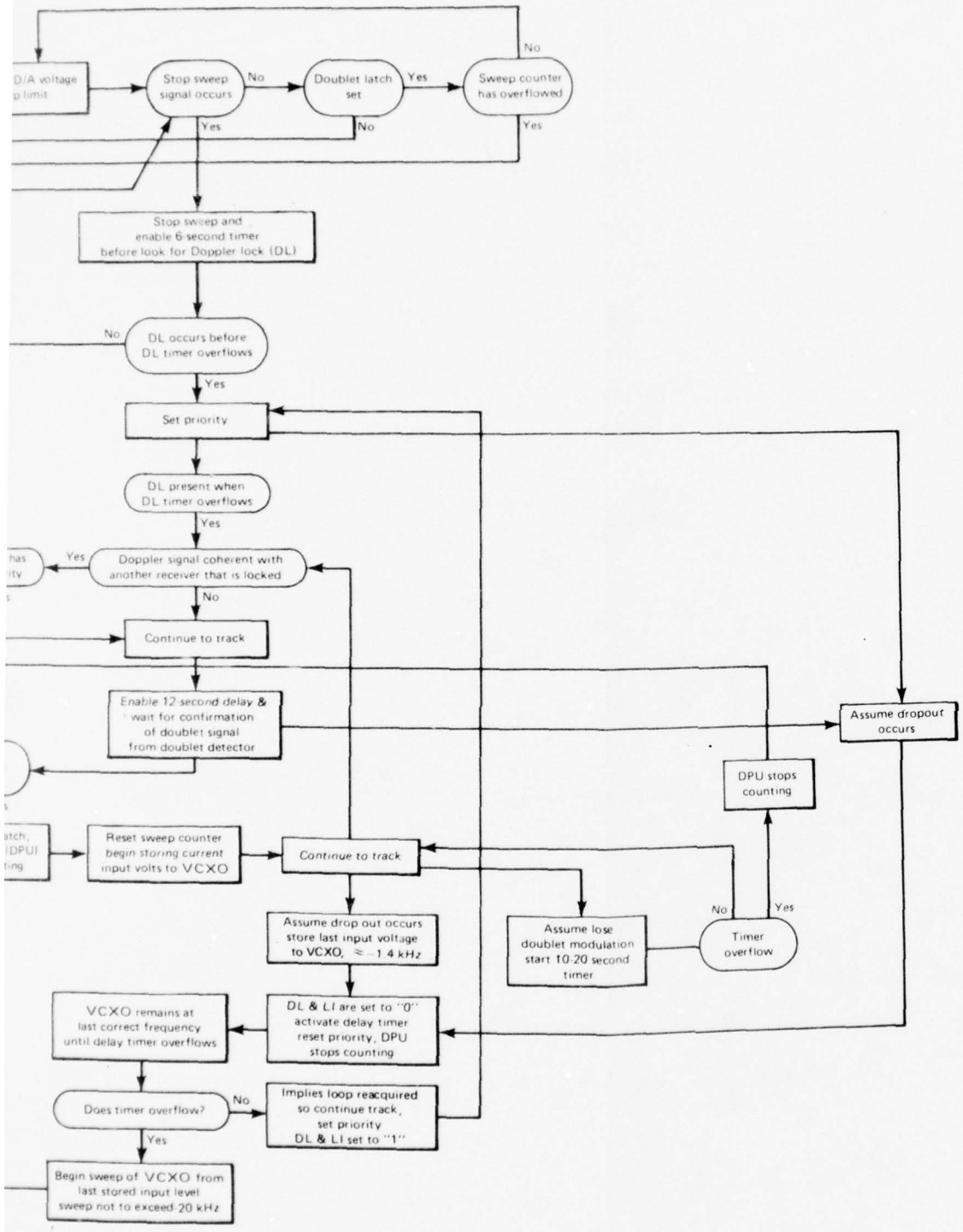


Fig. 18 Flow Diagram for 400-MHz Acquisition

is continued. If the loop loses lock while it is in the track mode, the DPU is informed of that event and another timer starts. If the loop does not reacquire the signal before this timer overflows, the search pattern is resumed.

High-Channel Controller. Because the HCPLL is the master channel, the control logic for the high channel is more complex than that for the low channel. Figures 19 through 24 illustrate the types of signal configurations the high-channel controller must accommodate. These figures represent Doppler frequency at 400 MHz versus time. The 0-Doppler axis represents the closest-approach or center-of-pass frequency. The positive or + Doppler region is defined as the satellite "rise" region, which can begin 20 kHz above the 0-Doppler axis. The negative or - Doppler region is defined as the satellite "set" region, which can extend to 20 kHz below the 0-Doppler axis.

Figure 19 illustrates the sawtooth search pattern of the high channel. The search time is about 40 s (corresponding to a search rate of 500 Hz/s) and the reset interval is about 1 s. This pattern is continued until an output from the stop-sweep detector stops the sweep, closes the loop, and starts an internal timer. If the loop does not acquire a signal before the timer overflows, it is because a false alarm has occurred and the search pattern will be resumed. When a false alarm occurs, the loop is opened and the sweep resumes, but the stop-sweep detector output is disabled until the search frequency has changed about 1.4 kHz away from the frequency of the false alarm. The initial search region is constrained to the region between +20 kHz and the 0-Doppler axis.

Figure 20 shows what occurs if the HCPLL tries to lock on a non-NAVSAT signal during the initial search period. The characteristics of the phase modulation of the NAVSAT signals are such that a square wave at about 101.7 Hz is present as a demodulated signal at the output of the high-channel auxiliary phase detector. If such a signal does not exist at the output of the auxiliary phase detector after the loop has been locked for about 12 s, the signal is defined as a "bogey." When this occurs, the loop is opened and the sweep resumes. The stop-sweep detector is disabled until the VCXO frequency has been changed about 1.4 kHz. The search region is still constrained to the region between +20 kHz and the 0-Doppler axis.

To detect the NAVSAT modulation, a narrow bandpass filter centered at 101.7 Hz is implemented by using a four-pole commutating filter. This is a device that basically requires a four-pole

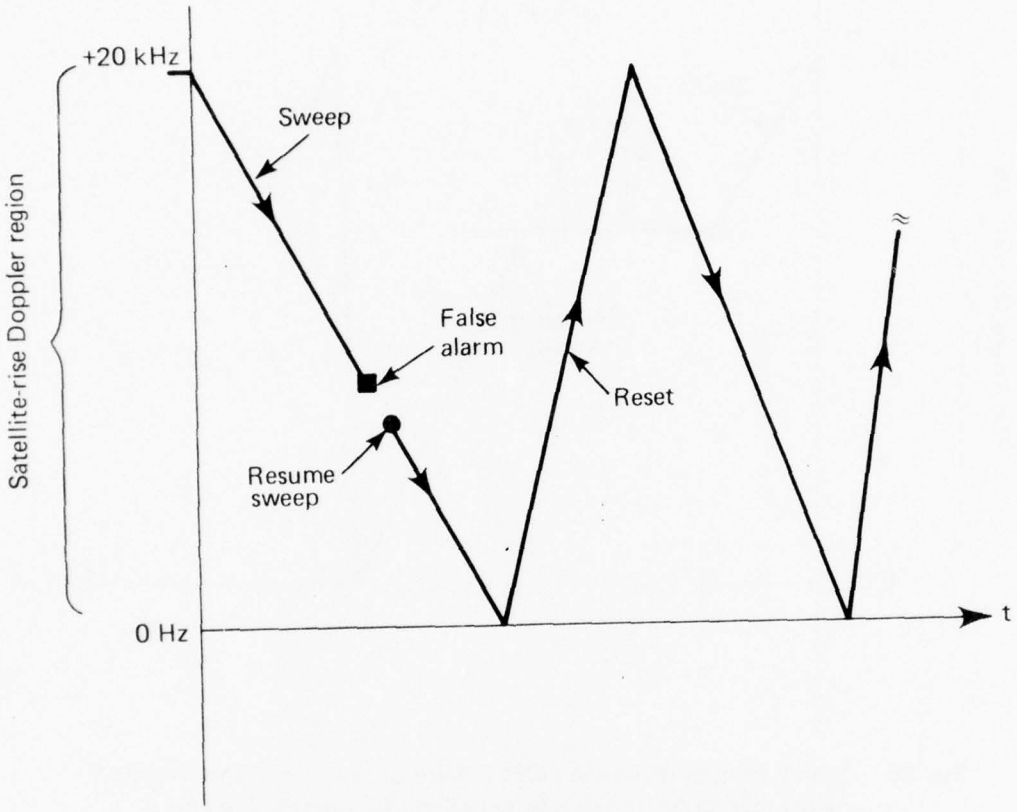


Fig. 19 Sawtooth Search Pattern of the High-Channel. (False alarm: no signal present but noise triggered stop-sweep detection circuit.)

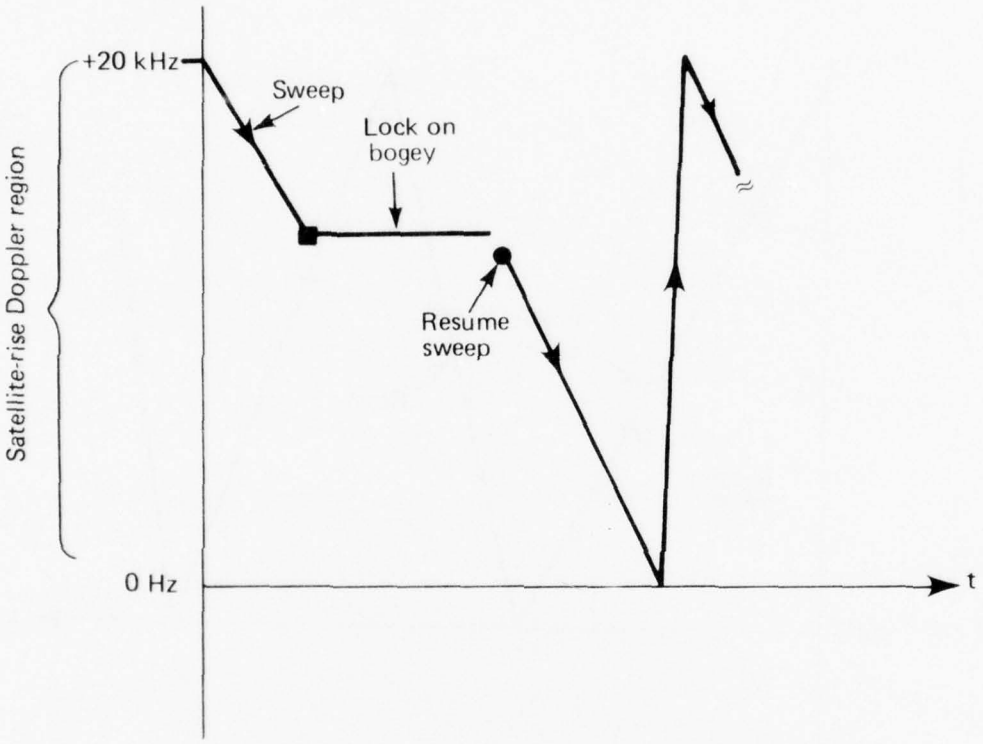


Fig. 20 Search Pattern When the HCPLL Tries to Lock on a Non-NAVSAT Signal During the Initial Search Period. (While searching for a NAVSAT, receiver locked onto signal at 400 MHz without "proper" modulation.)

analog commutator, a resistor, and four equal-valued capacitors. The 3-dB bandwidth of such a filter is

$$BW = \frac{2}{NRC},$$

where

N = number of poles in the commutator,

C = capacitor value, and

R = resistor value.

The Q of the filter (center frequency divided by BW) is seen to be a direct function of the RC product for a fixed N value.

$$Q = \frac{f_{center}}{2/NRC} = \frac{f_{center}}{2} \times NRC \ .$$

The desired center frequency is the 101.7-Hz clock rate, which is achieved by driving the commutator with a four-phase clock at 101.7 Hz derived from the NAVPAC stable oscillator. Each phase of the clock selects one pole of the commutator.

Figure 21 illustrates the operation of a DTL that has acquired and verified a NAVSAT signal, and has tracked the signal for some time. A loss of signal (perhaps because of an antenna null) is then assumed. When this occurs, a six-second timer is started, and the loop remains closed. If the signal reappears, the loop will reacquire the signal and tracking will continue. If the loop does not reacquire the signal before the timer overflows, the loop will open and the sweep will resume. While the loop was tracking the NAVSAT, the control logic was monitoring and storing the input to the VCXO (i.e., the frequency control voltage) to determine a starting frequency for the sweep. When the loop does not reacquire the signal before the timer overflows, the information is changed so that the starting frequency is retarded (instead of advanced as for a false alarm); e.g., if the last tracked frequency was +4 kHz, the starting frequency will be retarded to about +5.4 kHz relative to the closest-approach frequency. The new search area will be a 20-kHz region from +5.4 kHz to -14.6 kHz relative to the 0-Doppler axis. This region will be searched four times. If the signal is not reacquired, the control logic resets the search to the original rise region of +20 kHz to 0 Hz. The search region will not go below -20 kHz relative to the 0-Doppler axis. If the last tracked frequency should happen to be -10 kHz, the starting

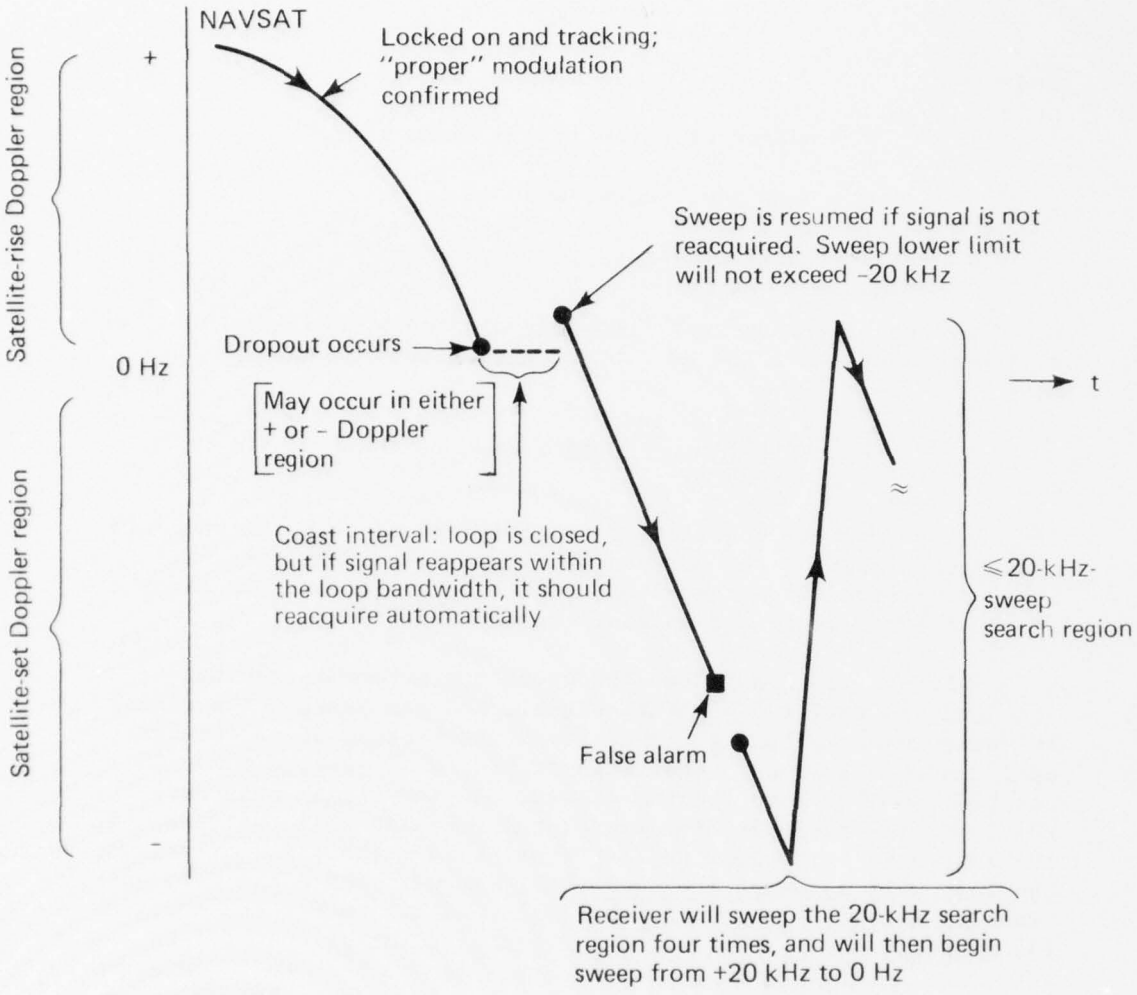


Fig. 21 Search Pattern After a DTL Has Acquired and Verified a NAVSAT Signal. (*Signal dropout (lost lock): receiver was tracking a signal that faded.*)

frequency would be defined as -10 kHz + 1.4 kHz = -8.6 kHz. The end of the search pattern would still be -20 kHz for a total search region of 11.4 kHz.

Beginning with NAVPAC Flight Unit 2 the control logic was modified to eliminate an undesirable characteristic. Figure 21 shows a false alarm being detected in the new search region. Beginning with Flight Unit 2, a false alarm detected in a new search region is handled like a false alarm in the initial search region; i.e., after the loop begins to sweep again, the fact that a false alarm occurred will not change the search region. In the control electronics of Flight Unit 1 this false alarm established a new starting frequency relative to the frequency of the false alarm.

One of the many problems that the NAVPAC system must contend with is when two DTL units acquire the same 400-MHz signal. Figure 22 illustrates a situation where DTL 1 has been tracking a NAVSAT signal, and then DTL 2 begins to track the same signal. The priority and coherency logic (PCL — electronics separate from the DTL) will have previously assigned DTL 1 priority over DTL 2 because DTL 1 began tracking the signal first. When DTL 2 begins to track the same signal, the Doppler frequencies from DTL 1 and 2 will be compared. Because they are equal and because DTL 2 has the lowest priority, it will be forced to continue in a search mode in the region of +20 kHz to 0 Hz until it locks onto a signal that is different from that tracked by DTL 1.

Figure 23 is a combination of the cases described by Figs. 20 and 21. As in the case of Fig. 21, the bogey does not change the search region defined after the loss of lock (beginning with System C2). A bogey establishes a new starting frequency in the Flight Unit 1 electronics.

In Fig. 24, DTL 1 (I) and DTL 2 (II) are tracking two different NAVSATs. In this example, II is assumed to have begun tracking first and therefore has priority over I. It is possible for the Doppler curves to "cross" (depending on the orbit configurations). When crossing occurs, both DTL units may suddenly begin tracking the same NAVSAT (either the I' II case or the I II' case). If the I II' case occurs, the second NAVSAT may never be reacquired by DTL 1 after it is forced to begin a new search pattern. In the I' II case, however, DTL 1 should reacquire the NAVSAT it was originally tracking.

The combinations of Figs. 18 through 24 are almost endless, but the examples given represent the major ones.

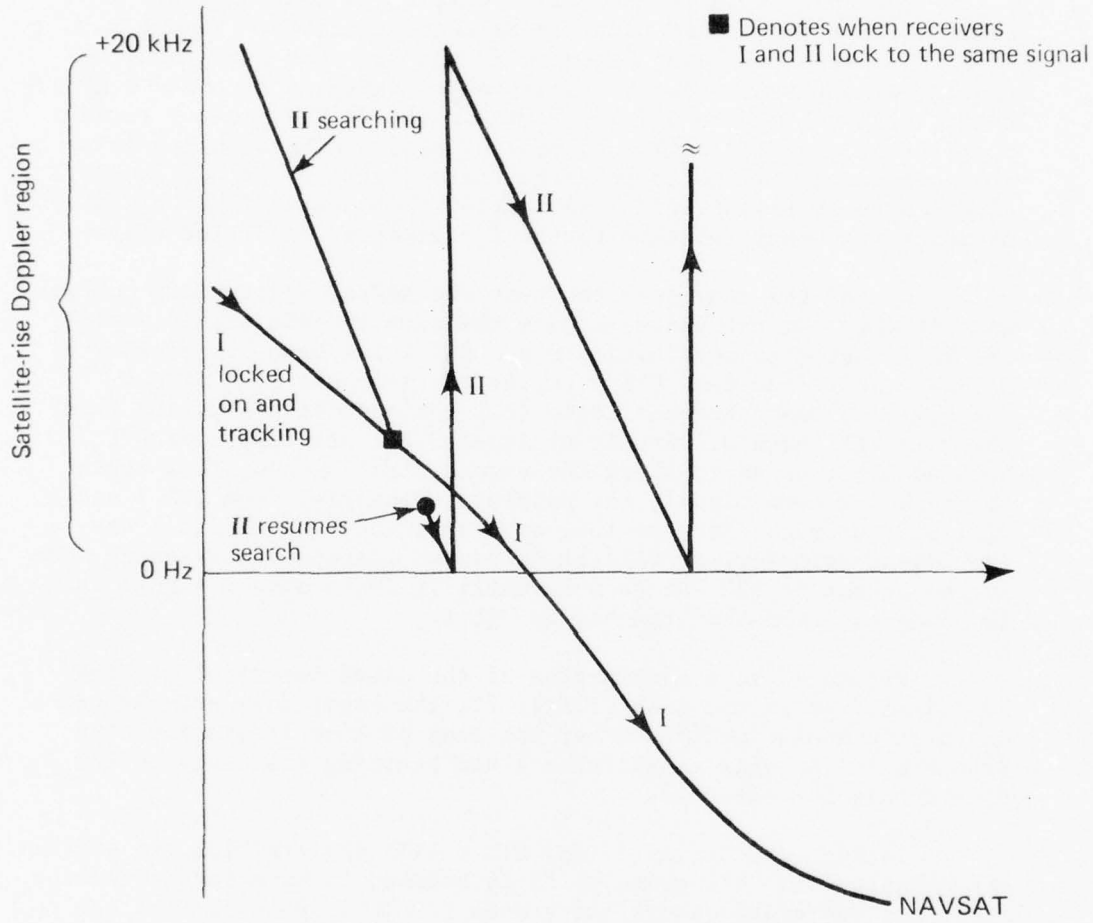


Fig. 22 Search Pattern When Two DTL's Have Acquired the Same 400-MHz Signal. (Two receivers locked on the same NAVSAT signal, but receiver I had higher priority.)

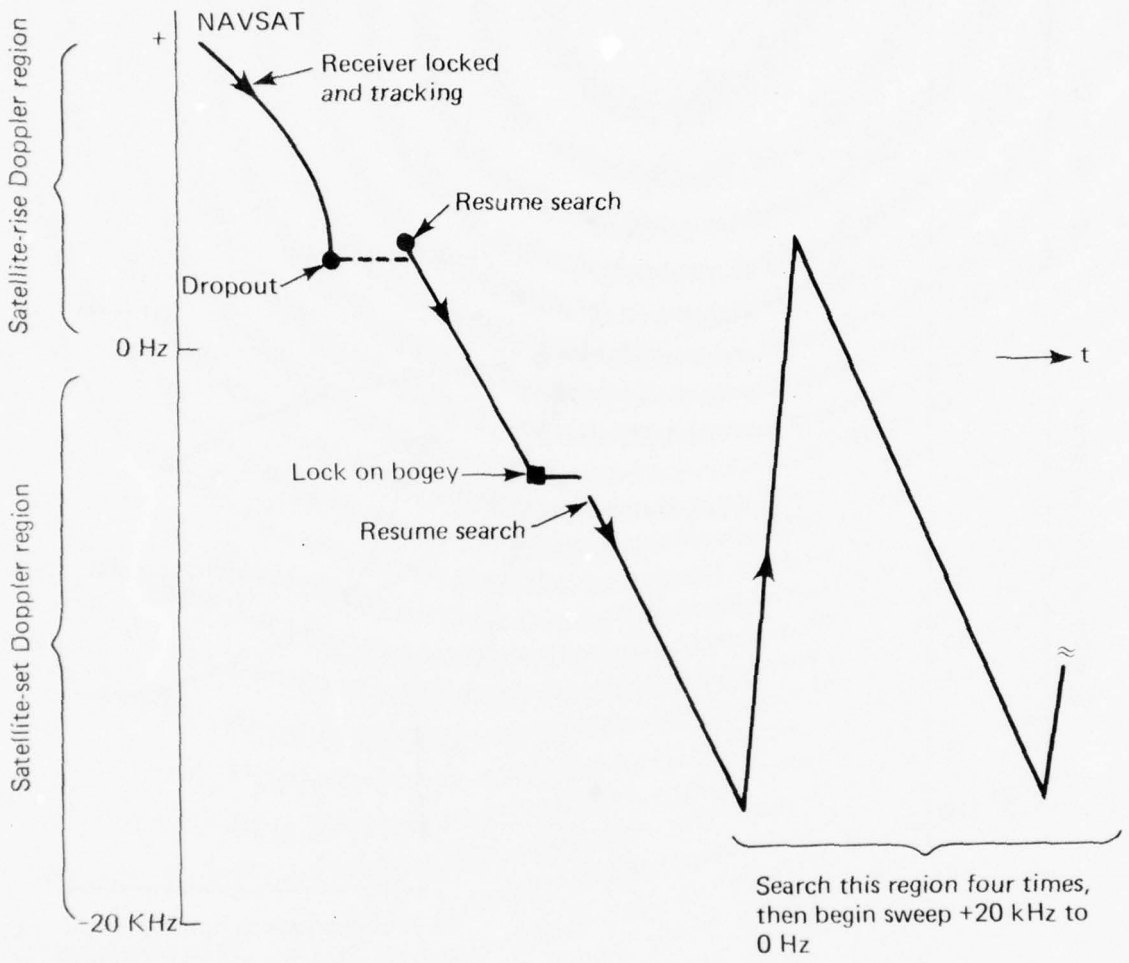


Fig. 23 Search Pattern When a Combination of Cases Described in Figs. 20 and 21 Occurs. (Receiver was tracking a NAVSAT, lost lock and then began search and locked onto strong signal without "proper" modulation.)

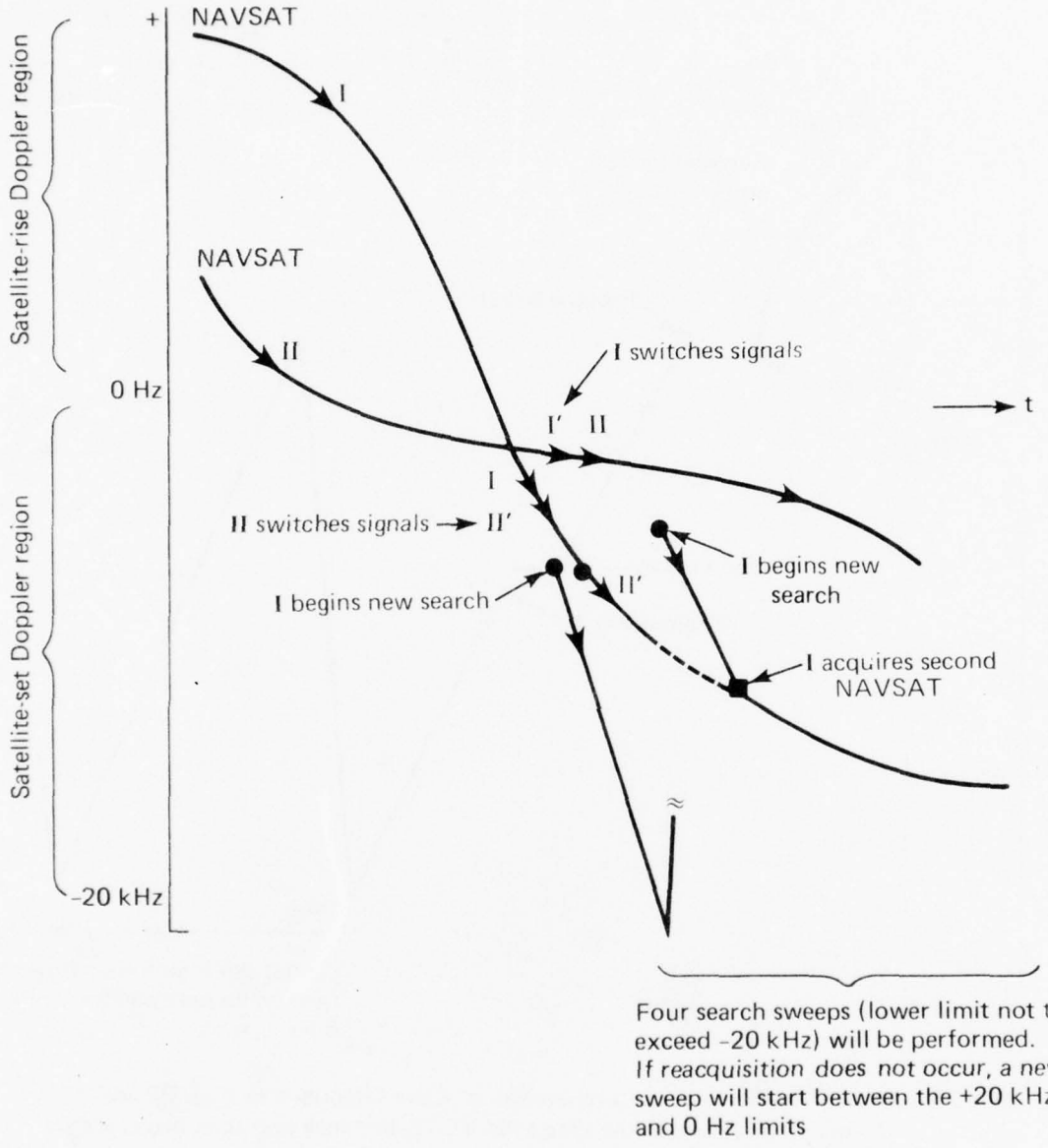


Fig. 24 Search Pattern After DTL 1 and DTL 2 Have Been Tracking Two Separate NAVSAT's. (Two receivers tracking two separate NAVSAT's. When Doppler signals cross, both receivers lock on same NAVSAT. Receiver II has highest priority (arbitrary definition for this example).)

High- and Low-Channel Second IF Amplifiers

Those portions of the NAVPAC DTL's called the second IF's perform more functions than just IF gain. Each unit contains a voltage-controlled attenuator to provide AGC. Each unit also contains the second mixer, the IF amplifier, and the IF crystal filter that limits the overall bandwidth. The low-channel unit provides two equal-power outputs to drive phase detectors. The high-channel unit not only provides two equal-power outputs to drive phase detectors, but a third equal-power output is provided (internal to the unit) that is passed through a narrowband crystal filter and amplitude detected. The amplitude-detected signal is output as a stop-sweep signal. (A summary of all the design characteristics is given in Table 6.) A block diagram of each is also included (Figs. 25 and 26).

It was desired that the delay variation of the NAVPAC receiver as a function of signal strength be minimized; i.e., for AGC control a constant-impedance attenuator should be used instead of simpler techniques such as transistor bias changes or shunt diodes across the signal path. The circuit chosen for the attenuator is a π configuration using HP-5082-3004 PIN diodes in each of the three legs. The impedance of a PIN diode is resistive and proportional to the current through it. Therefore, the π network can be made to look like a resistive attenuator and will have a constant impedance if the legs of the network, R_1 and R_2, can be made to satisfy the equation $R_1 R_2 = R_0^2$ (where R_0 is the network terminal impedance (50 Ω in this case)). To make the π network look like a resistive attenuator, the same bias current from a variable current source was run through both shunt diodes and summed with the current run through the series diode. As the current in the series diode varies, the current through the shunt diodes varies in the opposite direction to maintain a constant current through the summing resistor. A single-section attenuator such as this provides about 30-dB attenuation over the control range, but this was not sufficient dynamic range for NAVPAC; therefore two sections were placed in cascade such that the same bias current went through the diodes in both sections. The cascaded circuit provided about 60-dB attenuation over its control range with about 2.5- to 3-dB insertion loss. It was possible to use the same design in both the high and the low channels because stray reactances resulting from layout were the major frequency-determining elements.

There are three crystal filters used in the two units: the high-channel IF and stop-sweep filters, and the low-channel IF filter. All three are single-pole filters using average grade

Table 6

Design Characteristics of the Second IF Amplifier

Parameter	High Channel	Low Channel
RF frequency	64 MHz	24 MHz
LO frequency	61 MHz	22.875 MHz
LO input power	+6 dBm	+6 dBm
IF frequency	3 MHz	1.125 MHz
Overall net gain	63 dB	58 dB
IF bandwidth (IF crystal filter)	1200 Hz	300 Hz
Stop-sweep bandwidth (crystal filter)	60 Hz	-
Outputs:		
IF frequency	2 equal-power outputs	2 equal-power outputs
Stop-sweep detector	140 mV peak (typical open circuit voltage at -10 dBm output and room temperature)	
Image rejection	4 dB	9 dB
1-dB compression	0 dBm	0 dBm
Impedance (RF ports)	50 Ω	50 Ω
AGC control voltage (min. atten. at +13 V)	+13 to 0 V	+13 to 0 V
AGC control current (min. atten. at 1.5 mA)	1.5 to 0 mA	1.5 to 0 mA
AGC dynamic range	>60 dB	>60 dB
Power supply voltage:		
IF amplifier	-13 V	-13 V
Attenuator bias	+13 V	+13 V
Power supply current:		
IF amplifier	12 mA	12 mA
Attenuator bias	1.5 mA	1.5 mA

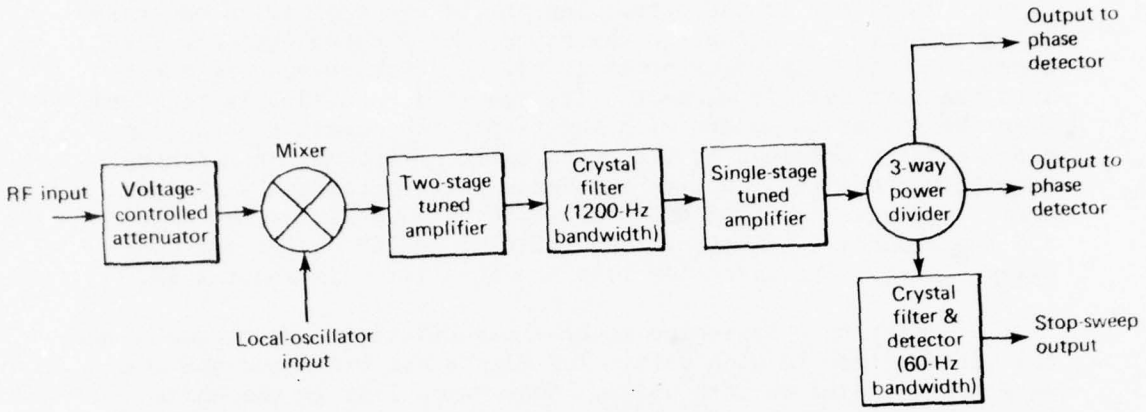


Fig. 25 Block Diagram of the High-Channel Second IF Amplifier

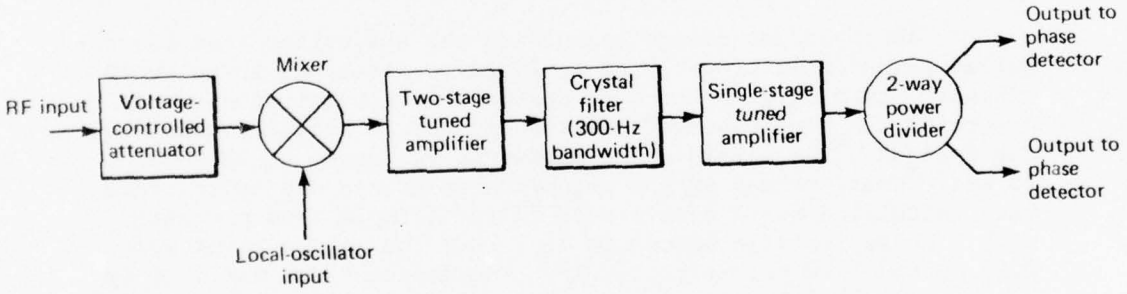


Fig. 26 Block Diagram of the Low-Channel Second IF Amplifier

crystals. The configuration of each filter is the same. A split-phase matching transformer is used to match the 50 Ω to the required impedance, which is dependent upon the specified bandwidth. The crystal is placed in one output leg of the transformer, a neutralizing capacitor is placed in the other, and the two legs are then summed. A matching transformer is placed at the output to match into the next circuit element. The required bandwidth is realized when the filter is loaded with the proper impedance, the real impedance being obtained by the turns ratio of the output matching transformer and the reactive impedance being obtained by transformer tuning. The bandwidths are 1200 and 300 Hz for the high- and low-channel IF filters, respectively, and 60 Hz for the stop-sweep filter. The insertion loss of each filter is about 2 dB.

A miniature low-noise double-balanced mixer was chosen to be the second mixer in each unit. The mixers are broadband and the same type is used in both units. Conversion loss in the units chosen is about 6 dB. For logistic reasons, these mixers, those used in the first IF amplifiers, and the power dividers used at the outputs were purchased from the same manufacture.

The losses from the attenuator, mixer, and crystal filter of each unit add up to about 11 dB. The high channel has a three-way power divider at its output, bringing the total losses to about 16 dB, while the low channel has a two-way power divider at its output, bringing the total loss to only 14 dB. Division of overall receiver gains is such that the required net gains are 63 and 58 dB for the high and low channels, respectively. Calculations then provide the required amplifier gains of 79 and 72 dB for the high and low channels, respectively.

The amplifier design began with the assumption that the required gains could probably be realized by cascading three tuned stages. Starting with the high channel, a calculation was made to determine the single-stage bandwidth if a 0.5% overall bandwidth was desired. The single-stage bandwidth was found to be about 30 kHz. Next, values of the required inductance and capacitance were calculated for a single-pole filter (simple tank circuit) with a characteristic impedance of 1 kΩ. The values found were 0.52 μH and 5410 pF, respectively. The inductor was realized by winding a toroidal coil with the best approximation resulting from 12 turns of No. 20 copper wire on a Micrometals T37-6 core; the average value obtained was 0.5 μH with a Q of approximately 170. A single-stage test circuit was built using a K2117 transistor to see whether the desired parameters could be obtained. At first the results were discouraging, but it was discovered that the tank-circuit capacitors were limiting the Q. However, when high grade capacitors were selected, a bandwidth of 50 kHz and 26-dB gain

were obtained. With these results, work proceeded based on a three-stage amplifier having an overall bandwidth that was going to be closer to 1% instead of the originally assumed 0.5%.

The three-stage engineering model of the amplifier was built before it was realized that the dynamic range (power delivery capability) of the final stage had been overlooked. With an overall bandwidth of 30 kHz, the final stage would have to deliver +11 dBm of rms noise power under normal conditions. This amount of power was incompatible with the power supply voltages already selected, the power consumption estimates, and the power levels of the reference signals used to drive the phase detector. Therefore, it was decided to place the IF crystal filter between the second and third stages. This reduced the required rms noise power delivered by the last stage to -3 dBm. Also, the final stage was rebiased to provide a 1-dB compression point of 0 dBm without requiring changes in the power supply.

The design pattern of the low channel was the same as that of the high channel. The circuit values for the tank circuit were scaled by a factor of 8/3 because the low channel is slaved to the high channel. In both high and low channels, a small part of the emitter resistance is unbypassed to provide negative feedback for overall gain adjustment.

The construction of the two units is identical. Each unit is built in an aluminum chassis having pieces that were dip brazed together. Shields within the enclosures isolate the input and output of each transistor stage. The brazed pieces are soldered on printed circuit boards that are, in turn, mounted to standoffs brazed into the chassis. For convenience in the next higher assembly, the layout of the printed ciruit boards for the high and low channels are nearly mirror images. Tight fitting covers complete the RF enclosure.

PRIORITY AND COHERENCY LOGIC

One of the problems confronting the NAVPAC receiver system is how to determine whether any two of the DTL units (DTL 1, 2, or 3) are tracking the same spacecraft, and if so, what action should be taken to terminate this condition. Figure 27 is a block diagram of the electronics used to solve the problem.

The priority and coherency logic (PCL) consists of a test clock generator, three coherency test counters, priority assignment logic, and the necessary logic elements to combine the coherency

test results and priority assignments to provide output signals to each of the DTL units.

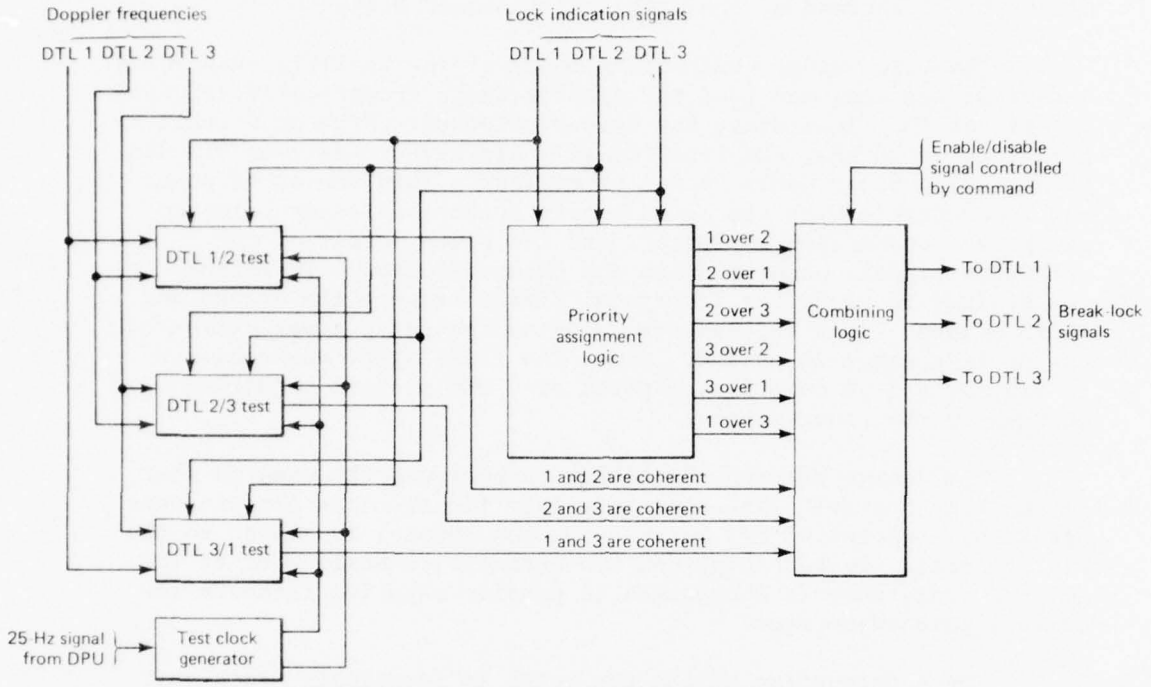


Fig. 27 Block Diagram of the Priority and Coherency Logic

Coherency Test Counters

Three separate test counters are used to measure the difference frequencies among the 400-MHz signals tracked by the DTL units. One counter tests the difference between DTL 1 and 2 frequencies, another tests DTL 2 and 3 frequencies, and the third tests the DTL 1 and 3 frequencies. If a difference frequency is 25 Hz or less, a decision will be made to force the lowest priority DTL to stop tracking the signal it is locked to and to begin a new search pattern. The coherency test is enabled as soon as any two DTL units have become locked to signals. The timing and performance of the coherency test is controlled by the test clock generator.

Test Clock Generator

The PCL receives a 25-Hz signal from the NAVPAC DPU. The signal is used to control the measurement intervals of the test

counters and to generate a signal that effectively repeats the coherency test once every 3.2 s. Because this signal is not synchronous with the time of Doppler lock of any DTL, the following events can occur:

1. If DTL's 1 and 2 were to lock to signals when the test clock had disabled the coherency counters, there would be a delay of up to 1.6 s before the first coherency test would be performed. After the first test (assuming the two frequencies differ by more than 25 Hz, i.e., not coherent) the coherency test would be repeated 3.2 s later.

2. If DTL 1 and DTL 2 were to lock to signals when the test clock had enabled the coherency counters, a coherency test would be completed within 0.2 s. If the two frequencies differ by more than 25 Hz, a second test would be performed after a delay of up to 3.2 s. After that, all subsequent tests are performed at 3.2-s intervals.

Priority Assignment Logic

Priority is assigned to the DTL units, based on the sequence in which they lock to signals. For example, if two spacecraft (S1 and S2) were in view and DTL 1 locked to S1 followed by DTL 2 locking to S2, DTL 1 would be assigned priority over DTL 2 and DTL 3, and DTL 2 would be assigned priority over DTL 3. If DTL 3 now locks to S1, the 3/1 coherency test will determine that the difference in Doppler frequencies between DTL 1 and 3 is less than 25 Hz and DTL 3 will be forced to begin a new search pattern. If the Doppler curves of S1 and S2 cross, DTL 1 and DTL 2 may suddenly begin tracking the same spacecraft. In this example, DTL 1 has priority over DTL 2, so DTL 2 would be forced to begin a new search pattern after coherency has been detected. However, if, at the time DTL 1 and DTL 2 began to track the same spacecraft, DTL 1 momentarily lost lock but then reacquired the signal, DTL 2 would be assigned priority over DTL 1 and DTL 1 would be forced to begin a new search pattern after coherency has been detected. Therefore, at any given time, the priority assignments can be 1 over 2 or 2 over 1, 1 over 3 or 3 over 1, and 2 over 3 or 3 over 2.

Combining Logic

When the result from one of the coherency test counters indicates that two DTL units are locked to signals whose difference

frequency is less than or equal to 25 Hz, priority assignment information and coherency test results are logically ANDed to generate a signal to the low priority DTL, requiring it to begin a new search pattern. Commands are included in the overall NAVPAC system to disable all PCL output signals to the DTL units. If this command state is chosen, it is possible for all three DTL units to track the same spacecraft simultaneously even though priorities have been assigned and coherency of signals is being detected.

7. DATA SYSTEM

The NAVPAC data flow diagram (Fig. 28) shows the movement of the data throughout the NAVPAC electronics. Everything in Fig. 28 except the three dual-channel receivers, the three-axis accelerometer, and the tape recorder is part of the NAVPAC DPU.

CENTRAL PROCESSING UNIT

At the heart of the DPU is the CPU, which accepts digitized data from various other subsystems of the DPU. The function of the CPU is to create several special data files of different types of data in a temporary buffer memory. When the buffer memory is full the contents are transferred to a tape recorder that can hold many buffer dumps. Later, the tape recorder can be played back while the host vehicle is over a ground station to transfer the data to the ground data processing system.

Figure 29 is the block diagram of the CPU. The CPU is similar to a standard stored-program digital machine, but with very little arithmetic capability. The stored programs and program constants are kept in a read only memory (ROM). The programs and the constants are selected by vectors generated by the logic in the priority and mode control systems, as well as by program control. For example, in each of three major modes the control logic selects a complete new set of program constants for the software to use.

The CPU accepts data serially and stores it in 16-bit bytes in a quarter-million bit random access memory (RAM). After each byte of data is stored it is only necessary to increment the address of the storage location by one and compare this address to the address of the "full" storage location to determine whether the file is full. Therefore, the only arithmetic functions required of the CPU are increment (add one) and compare (is $A \geq B$?).

In addition to data files, the CPU maintains a list of all the current-storage-location addresses (called pointers) in a special file referred to as the table of contents. Thus, before a data word can be stored in a particular file the CPU must fetch the current-storage-location address from the table of contents. At the completion of the data storage program, the latest storage location address must be returned to the table of contents.

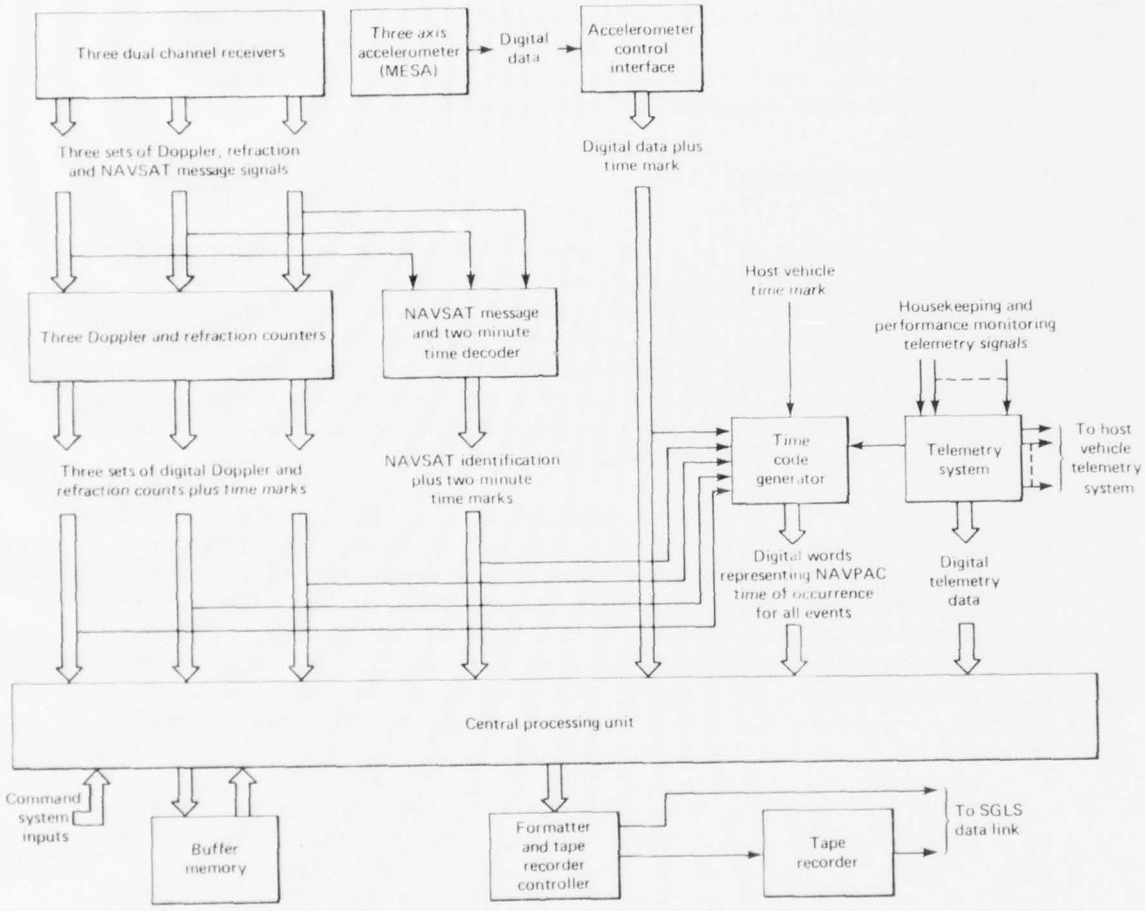
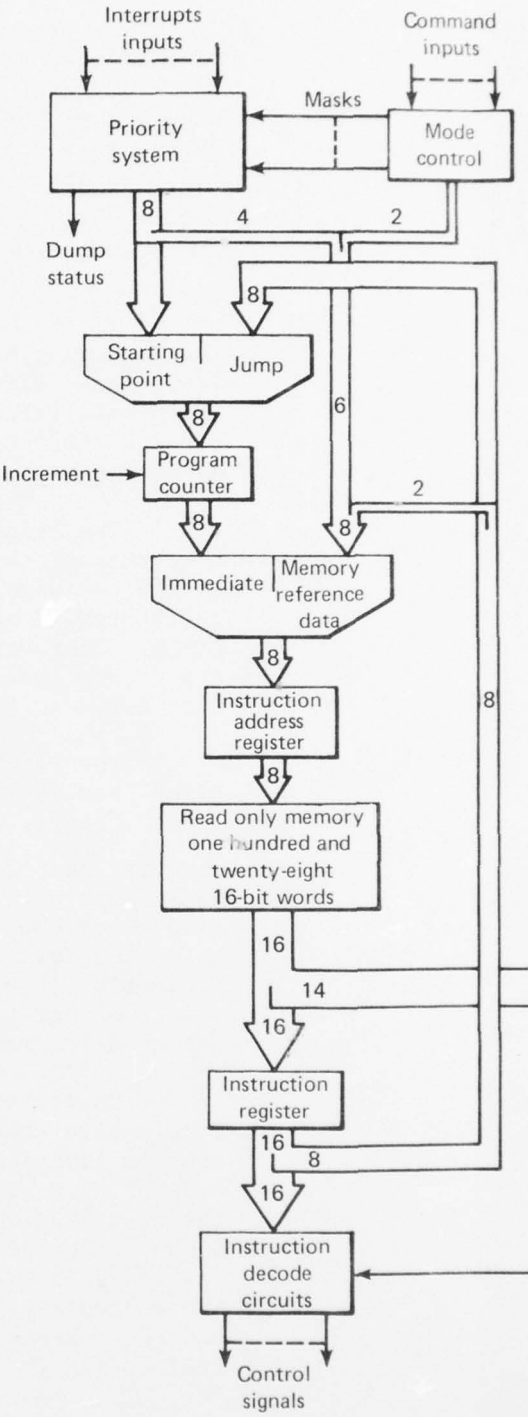


Fig. 28 Data-Flow Diagram of NAVPAC


Interrupts inputs
Command inputs
Masks
Priority system
Mode control
8
4
2
Dump status
8
Starting point
Jump
6
8
Increment
Program counter
2
8
8
Immediate
Memory reference data
8
Instruction address register
8
Read only memory one hundred and twenty-eight 16-bit words
16
14
16
Instruction register
16
8
16
Instruction decode circuits
Control signals

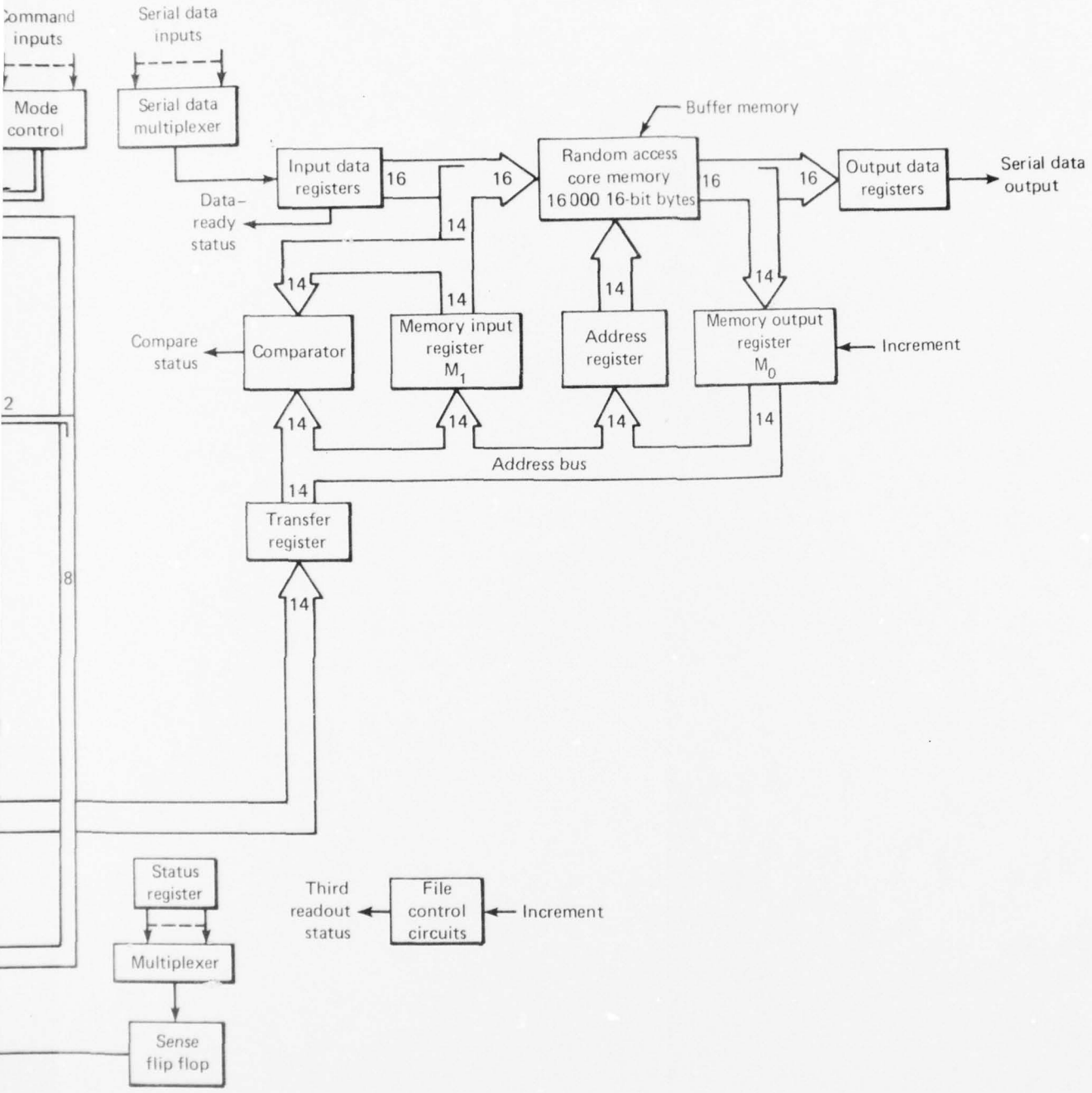


Fig. 29 Block Diagram of the Central Processing Unit

In brief, the CPU responds to interrupts from other subsystems of the DPU. It accepts from them serial digital data that it sorts and stores in special files that it maintains in a core RAM. When one of the files becomes full, the contents of the RAM are dumped in an orderly fashion to an external mass storage device (tape recorder).

File Maintenance

The CPU creates and maintains a file in the buffer memory in the following manner. At any one time the RAM contains four files, i.e., three data files and the directory or table of contents. The three data files contain data and time information pertaining to three different kinds of information: Doppler navigation data, accelerometer measurement data, and telemetry housekeeping data.

The structure of a file is shown in Fig. 30. We are not concerned at this point about what the data are that are being stored; we only want to keep track of where they are being stored. Therefore, we are interested in the addresses of the storage locations. There are three constants that define a file; these constants are the addresses of the three particular storage locations: TOF, BOF, and FFM (the key defines the terms).

TOF is the address of the very first storage location in a file. BOF is the address of the very last storage location in a file. Clearly $BOF_m + 1 = TOF_{m+1}$; that is, the top of one file is the very next location after the bottom of the previous file. The third constant is the file-full mark, FFM. When the data in the file reach the FFM, the file is considered full and dumping of the buffer is initiated. The difference, BOF - FFM, must be made sufficiently large to absorb all data at the maximum data rate during the time that the buffer is dumping, since data collection continues at all times, even during buffer dump.

There are two variable addresses that are required to maintain a file, EOF and SOF. EOF is the address of the first empty storage location in the file. It is the address where the next byte of data will be stored (see Fig. 30). SOF is the address of the next byte of data to be read out of the file during a buffer dump. Since EOF and SOF are variables, they must be stored in RAM (as shown in Fig. 30). They are stored in the table of contents. The addresses in the table of contents, AEOF and ASOF, are constants and these are kept in ROM along with the aforementioned constants that define the file.

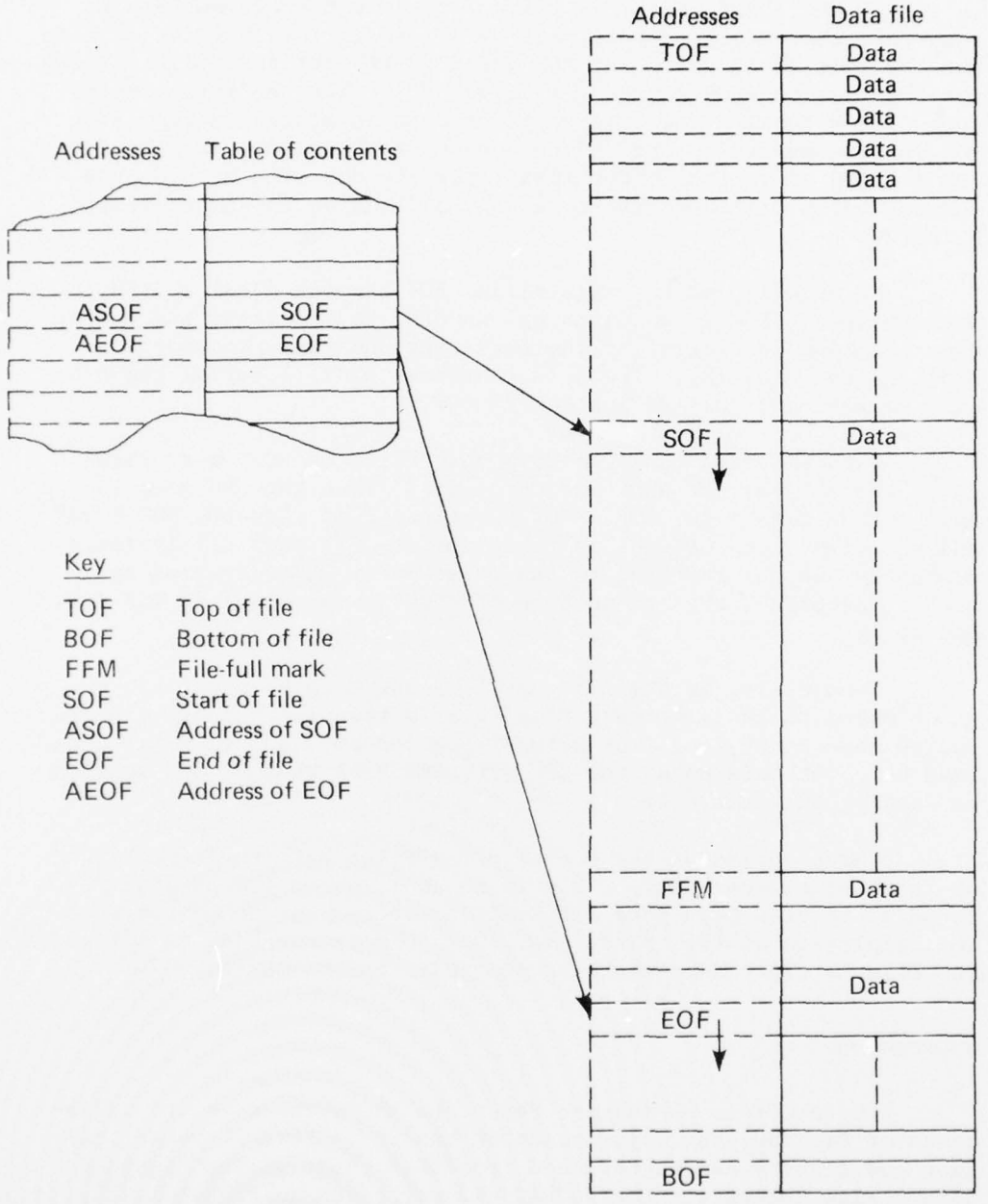


Fig. 30 File Structure in the NAVPAC Buffer Memory

Consider what happens as the file fills and empties during the course of data collection and buffer dump. Initially the file is empty, EOF = TOF and SOF = TOF. Each time the CPU answers an interrupt that requires that data be placed in this particular file, the CPU must first go to the ROM and get AEOF for this file. Then the CPU goes to AEOF in the RAM to get EOF. For the first interrupt, EOF = TOF and the first byte of data is placed in TOF; then EOF is incremented by one and the second byte of data is placed in TOF + 1 and so forth. After each interrupt has been served, the current value of EOF is restored to the location in RAM addressed by AEOF.

Eventually, as the file fills, EOF becomes equal to FFM. When the EOF = FFM is detected by the CPU, it initiates the buffer dump sequence controlled by the formatter and tape recorder controller (see Fig. 28). The file continues to fill during the process so EOF continues moving toward BOF.

When the time comes to dump this file, the CPU must first go to the ROM and get ASOF for this file. Then the CPU goes to ASOF in the RAM to get SOF. For the first dump request, SOF = TOF and the first byte of data is taken out of TOF; then SOF is incremented by one and restored to the location in RAM addressed by ASOF. Therefore, the second byte of data is taken out of TOF + 1, and so on.

Eventually, as the file empties, SOF becomes equal to EOF, which means there is no more real data in the file. There are of course some empty locations between EOF and BOF, but they are not read out. At this point the CPU sets SOF back to TOF, and goes on to dumping the next file.

Three copies of the buffer are written onto the tape recorder to provide redundancy. This is in addition to the parity, which is added to each data word before it is stored in the buffer. At the completion of the third dump, the CPU sets EOF back to TOF and the file is right back where it started: EOF = TOF and SOF = TOF.

Flow Charts

The previous subsection described in words, with the assistance of Fig. 30, the major tasks of the CPU. Further formalization and clarity can be obtained from flow charting the required jobs. Flow charts for the NAVPAC CPU are given in Figs. 31, 32, and 33. A detailed description of these flow charts will not be given since rereading the previous section while studying Figs. 31, 32, and 33 should provide ample information.

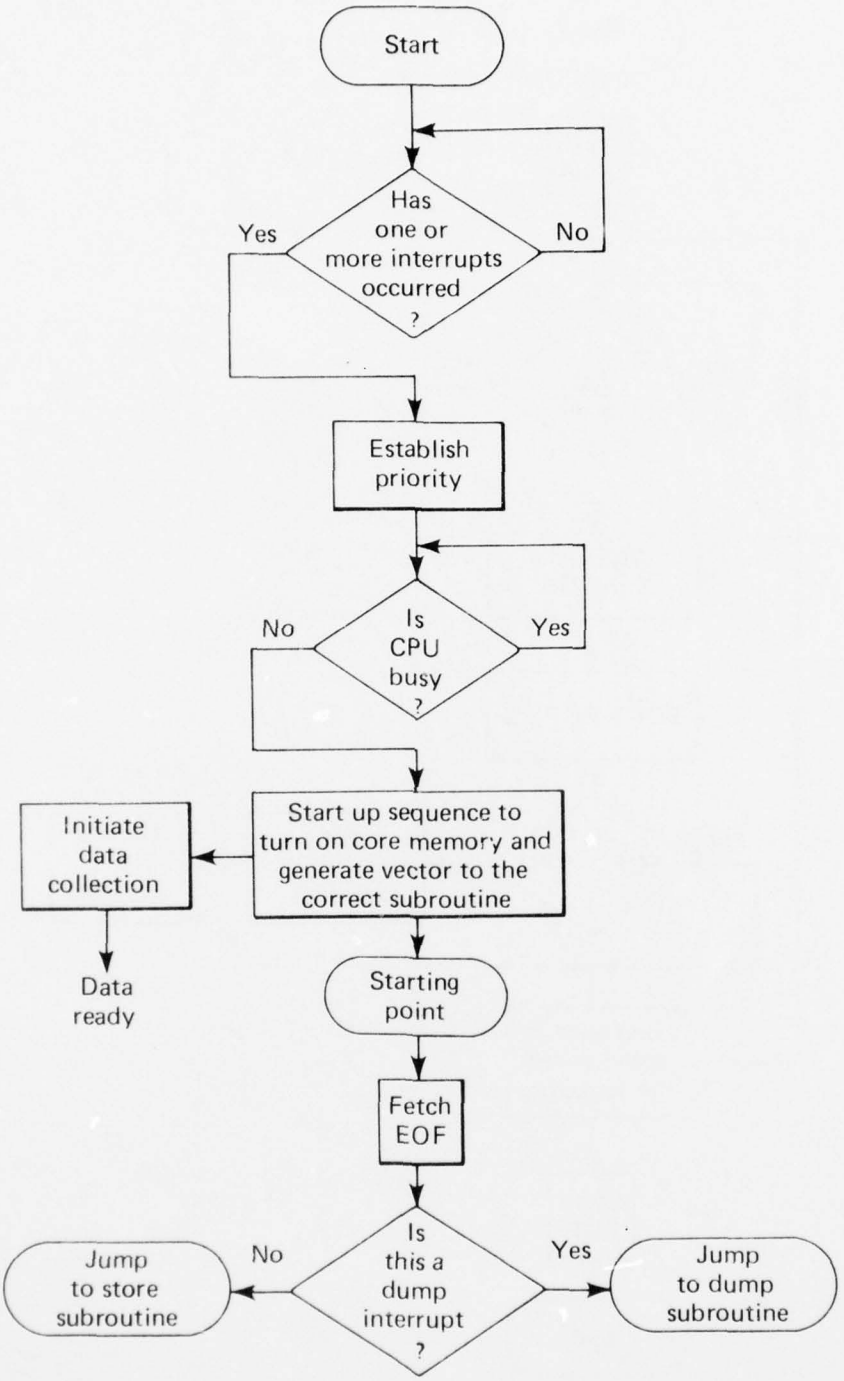


Fig. 31 Flow Diagram of the Start Sequence

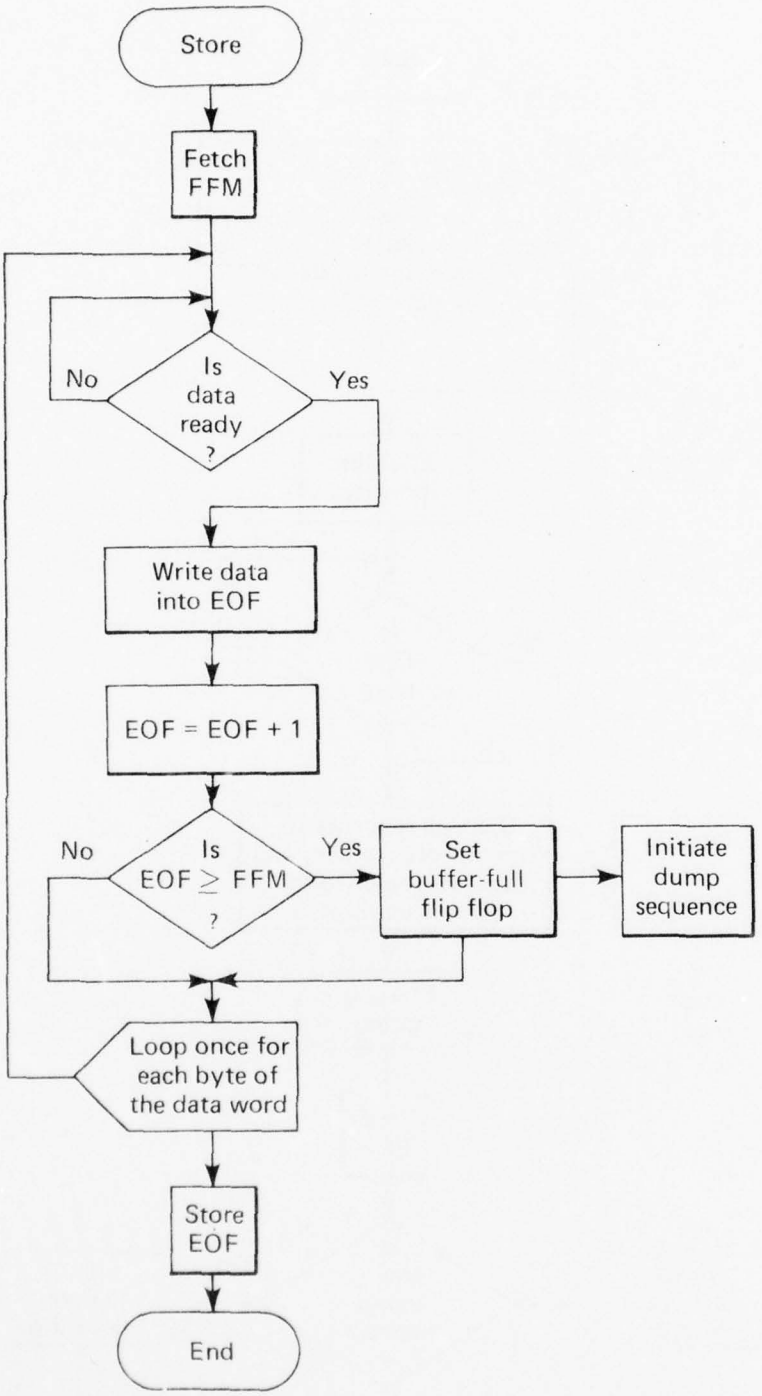


Fig. 32 Flow Diagram of the Store Subroutine

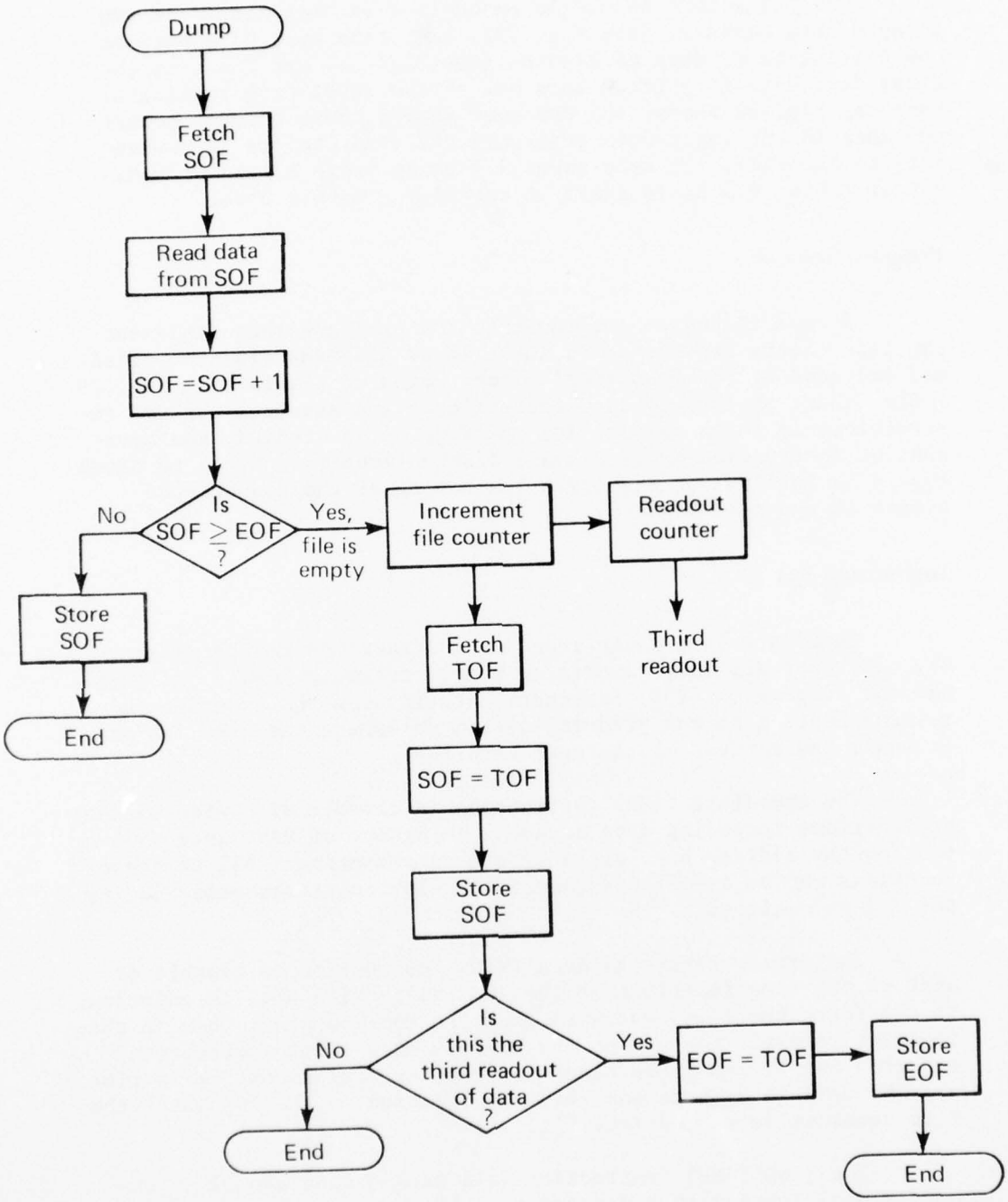


Fig. 33 Flow Diagram of the Dump Subroutine

One thing that should be emphasized is that since the CPU accepts data serially (see Fig. 29), some time must pass between the initiation of data collection (see Fig. 31) and the time the first data byte is shifted into one of the input data registers. Hence as Fig. 32 shows, the CPU must always check to see whether the data in the input data registers are ready before it writes data to the file. It only takes 7.2 μs to write a byte to RAM, but it takes 19.2 μs to shift in serially a 16-bit byte.

Program Control

It was discussed earlier that the programs that implement the flow charts are stored in ROM. These programs are controlled and executed by the functional blocks shown on the left in Fig. 29. A flow chart of the sequence that selects and executes the CPU instructions is shown in Fig. 34. As Fig. 34 is studied, the movement of instruction addresses and instructions from block to block should be followed on Fig. 29. The timing of the sequence of events is shown in Fig. 35.

Instruction Set

There are four basic types of instructions indicated in Fig. 34; they are end, immediate, memory reference data, and jump. The *end of program* (END) instruction terminates the programs and returns control to the priority system to select the next job or to await the arrival of the next interrupt.

The immediate (IMD) instruction is capable of a wide variety of functions including data movement in or out of RAM, data movement on the address bus, sensing, and incrementing. All of these functions can be executed sequentially with one instruction during one 7.2-μs cycle time.

The memory reference data (MRD) instruction is capable of most of the same functions as the IMD instruction and, in addition, it can fetch the file constants from the ROM and place them in the transfer register for use on the address bus. This instruction requires two 7.2-μs cycle times to execute. The second cycle time must be used to address and read the location in the ROM where the file constant is stored (see Fig. 34).

The jump (JMP) instruction will permit conditional or unconditional jumping to a new point in the program. A conditional jump will take place if the sense flip-flop has been previously set to the "1" state (see Fig. 34).

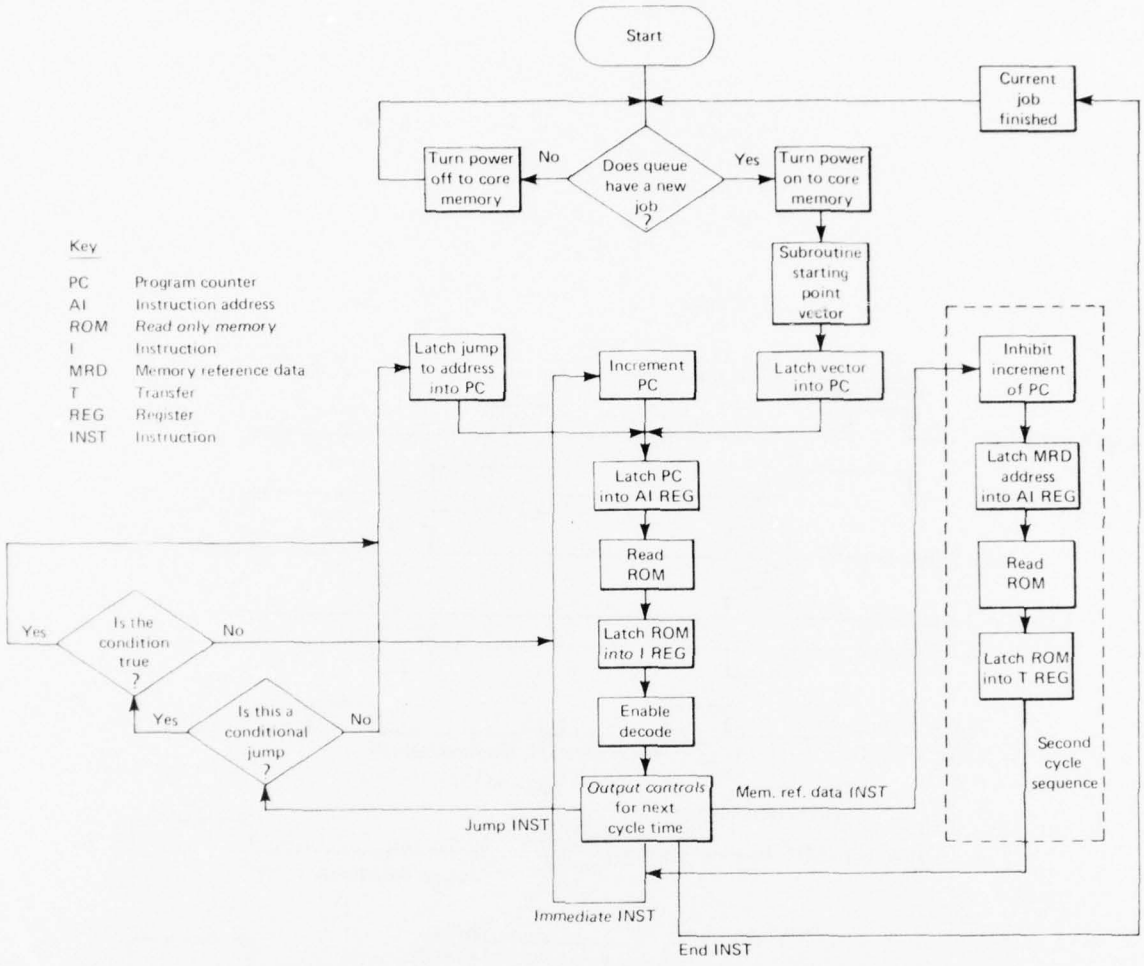


Fig. 34 Flow Diagram of the Instruction Sequence

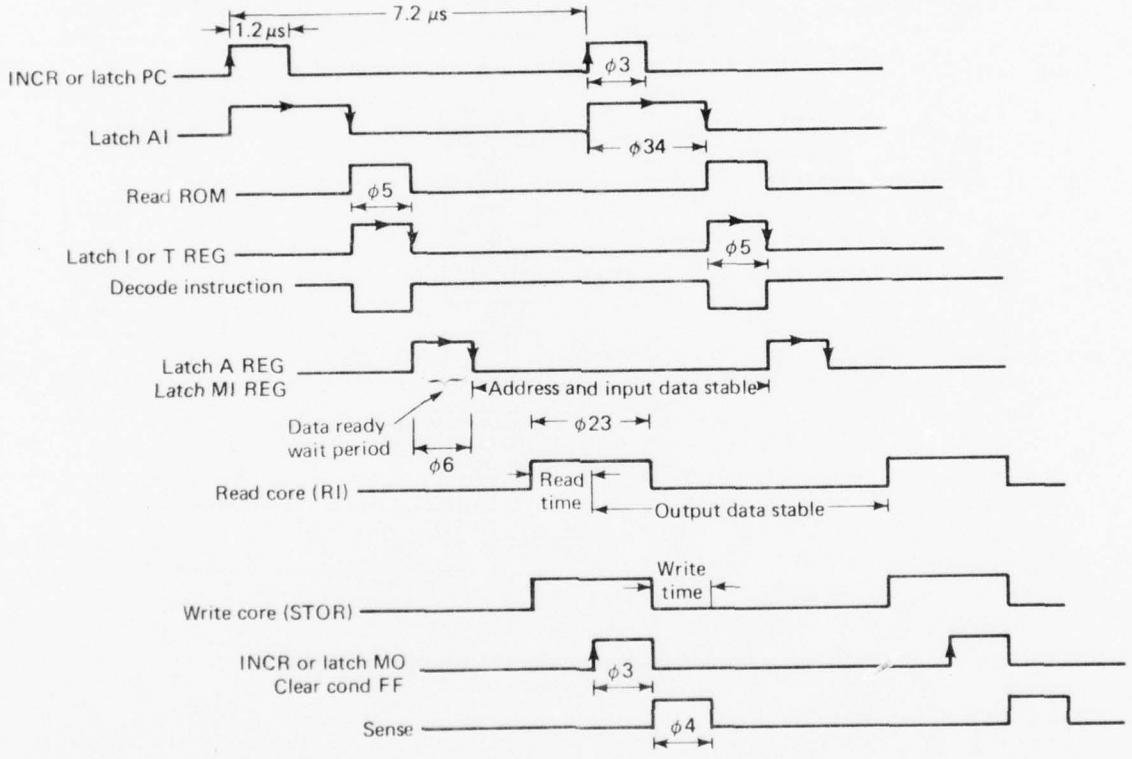


Fig. 35 Timing Diagram of the NAVPAC Central Processing Unit

The formats of the four types of instructions are given in Fig. 36. The functions of the I bits that make up the command field of the instruction words are given in Table 7. If the particular I bit is a logic 1, that function will be performed during the cycle time. The effect on data movement or address manipulation of each function listed in Table 7 can be followed and studied in Fig. 29.

A Sample Instruction

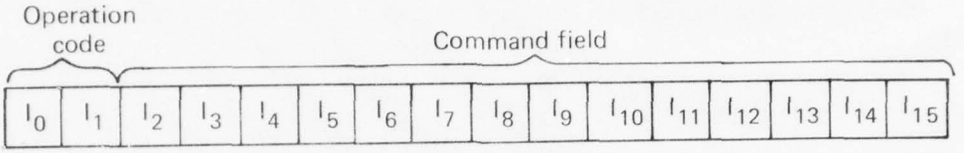
Consider the instruction 560A (in hexadecimal), which in binary becomes:

$$\underset{I_{15}}{0}\ 1\ 0\ 1\ 0\ 1\ 1\ 0\ 0\ 0\ 0\ 0\ 1\ 0\ 1\ \underset{I_0}{0}$$

Since $I_0 I_1 = 01$, this is an IMD instruction. Since I_2 is a zero, the memory output register (M_0) is driving the address bus. Assume that the memory output register contains EOF and that the memory input register (M_I) contains FFM. Follow the execution of this instruction in Fig. 29 and Fig. 35 (for timing) while referring to Table 7 for the I-bit code. I_3 is a 1 so at clock Ø6 (see Fig. 35) the address EOF will be latched into the address register. If the data input registers have no data, the CPU will wait in the Ø6 state until the data are ready. Then, since I_9 is a 1, the data will be written from the data input registers into the memory at location EOF during Ø2 through Ø4. In the meantime, since I_{10} is a 1, the memory-output register will be incremented by 1 during Ø3 and, since I_{12} and I_{14} are 1's, the output of the comparator will be latched into the sense flip-flop and the buffer-full flip-flop during Ø4. Notice that the comparator is comparing the new value of EOF with the value of FFM held in the memory input register (is EOF ≥ FFM?). Now refer to Fig. 32; notice that the one instruction (560A) that we have just considered is equivalent to one cycle through the major loop in the STORE subroutine. Three 560A instructions in a row will store a three-byte data word in a file.

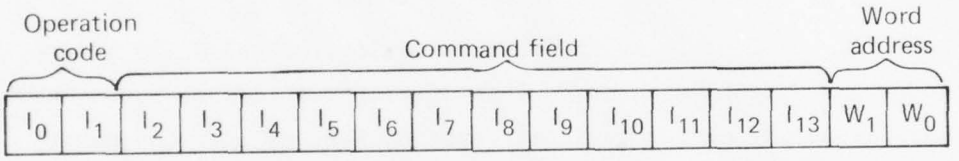
Read Only Memory Organization

To understand completely the use of MRD and JMP instructions, it is necessary to look at how the programs and file constants are

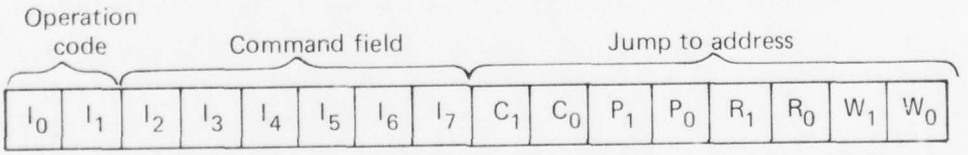


0 0 end of program, END

0 1 immediate, IMD



1 0 memory reference data, MRD



1 1 jump, JMP

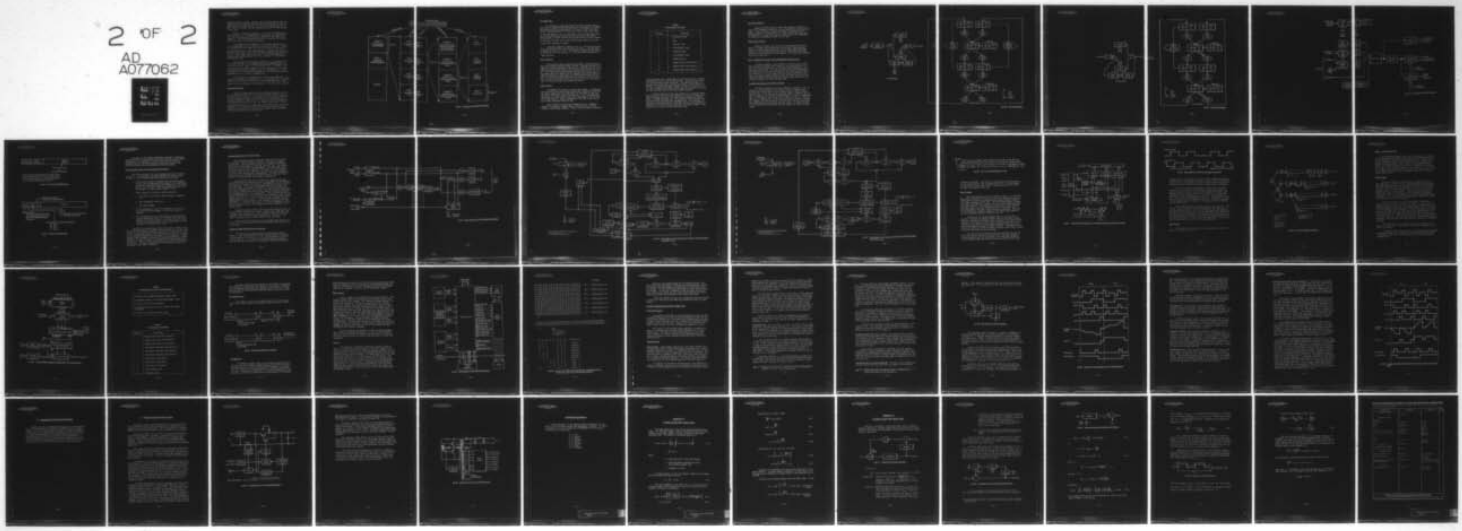
Fig. 36 Instruction Formats

Table 7
Instruction-Bits Code

I_2	address bus source: T register ($I_2 = 1$) or M_0 register ($I_2 = 0$)
I_3	latch address bus into address register
I_4	latch address bus into M_I register
I_5	read from memory into M_0 register
I_6	write from M_I register into memory
I_7	conditional bit: $I_7 = 1$, conditional jump; $I_7 = 0$, unconditional jump
I_8	read from memory into output data registers
I_9	write from input data registers into memory
I_{10}	increment the M_0 register
I_{11}	sense third readout status
I_{12}	sense-compare status
I_{13}	sense-dump status
I_{14}	if sense set buffer full flip-flop
I_{15}	if sense increment file counter

AD-A077 062 JOHNS HOPKINS UNIV LAUREL MD APPLIED PHYSICS LAB F/G 22/3
NAVPAC -- A SPACE-QUALIFIED NAVIGATION PACKAGE.(U)
FEB 79 D L ZITTERKOPF N00017-72-C-4401
UNCLASSIFIED APL/JHU/TG-1317 NL

2 OF 2
AD
A077062



END
DATE FILMED
12-79
DDC

organized within the ROM. Consider the 8-bit ROM address word implied in Fig. 29, shown as part of the JMP instruction in Fig. 36, and repeated in detail in Fig. 37. Since the present size of the ROM is only 128 words, the most significant bit of the ROM address is not used.

Figure 37 shows that chapter 1 of the ROM (the higher order addresses 40 to 7F in hexadecimal) is sequential in organization; i.e., the subroutines are packed one right after the other into chapter 1. The JMP instruction can move to any point in this part of ROM to pick up the required subroutine.

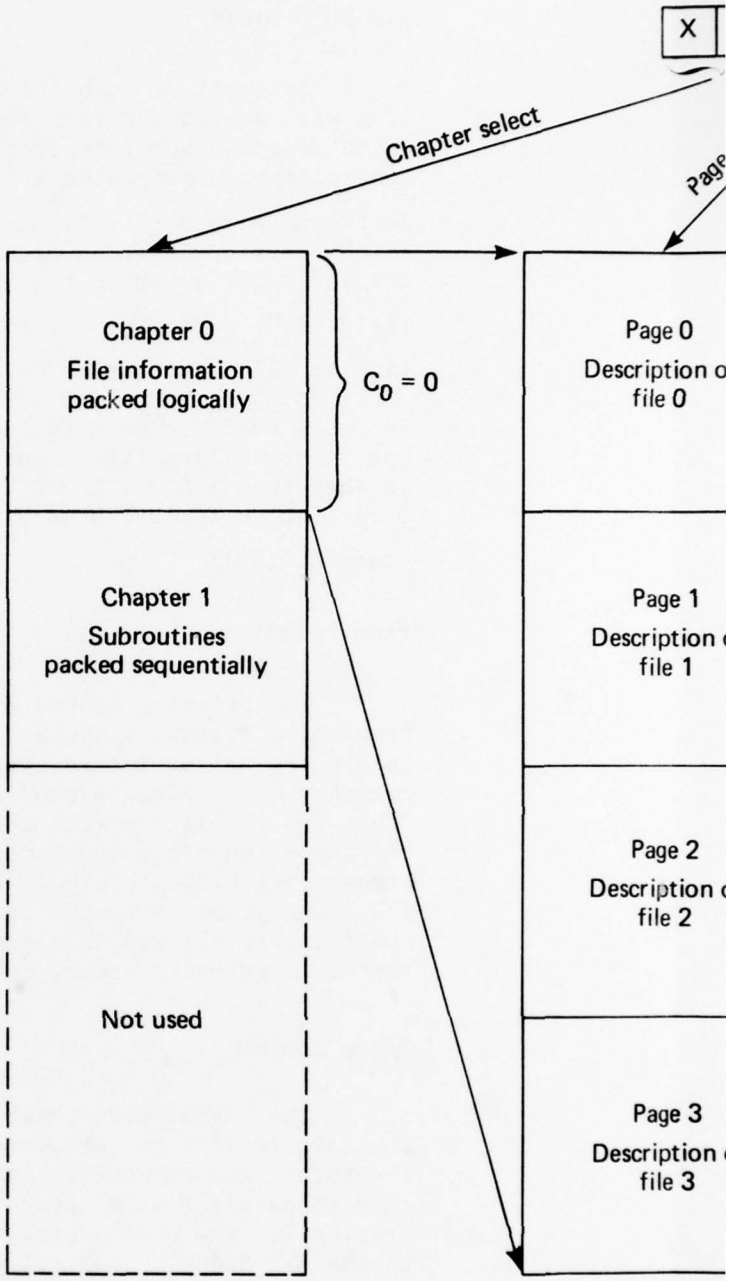
The organization of chapter 0 (lower order addresses 00 to 3F in hexadecimal) is very structured as shown in Fig. 37. Chapter 0 is divided into four pages that can be selected by bits P_1P_0 of the ROM address word. Each page contains a complete description of one particular file. File 0 is the directory or table of contents, file 1 is the Doppler data file, file 2 is the MESA (miniature electrostatic accelerometer) data file, and file 3 is the TLM (telemetry) data file.

The structure of each page is identical. For example, page 1, as shown in Fig. 37, is divided into four paragraphs that can be selected by bits R_1R_0 of the ROM address word. Paragraph 0 contains the starting point program for this particular file as shown at the bottom of the flow chart in Fig. 31. Paragraphs 1, 2, and 3 contain a list of the file constants for this particular file for operating modes 1, 2, and 3, respectively.

The structures of paragraphs 1, 2, and 3 are identical. For example, paragraph 2, as shown in Fig. 37, is divided into four words that can be selected by bits W_1W_0 of the ROM address word. These words are the now familiar file constants: TOF, ASOF, AEOF, and FFM.

Starting Point Vector

Figure 29 shows that the priority system generates a vector to the starting-point program for the file being called by the interrupt that is in effect. It was shown in the previous subsection that this program resides in paragraph 0 of the particular page devoted to that file (see Fig. 37). Therefore, the required vector is $X0P_1P_00000$, where P_1P_0 is the file number (in binary). Notice that any MRD instruction to fetch the file constants will also need to refer to this same page; hence the four most significant bits (MSB's) of this vector are also used to form the index from which the MRD instruction works (see Fig. 29).


X
Chapter select
Page
Chapter 0
File information
packed logically
$C_0 = 0$
Chapter 1
Subroutines
packed sequentially
Not used
Page 0
Description o
file 0
Page 1
Description
file 1
Page 2
Description
file 2
Page 3
Description
file 3

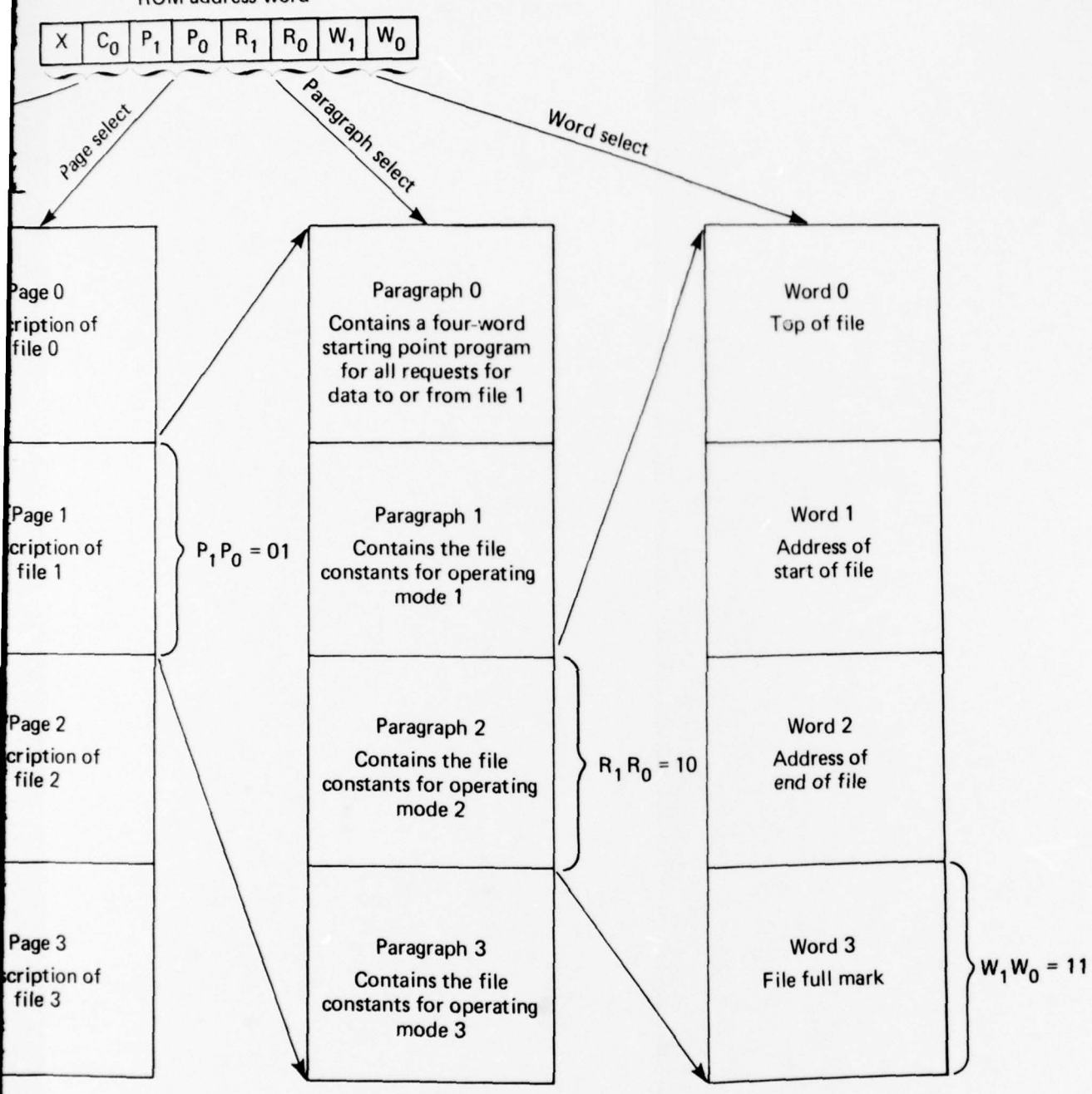


Fig. 37 Partitioning of the Read Only Memory

The MRD Index

To continue to build the index from which the MRD instruction will do index-relative addressing, it is necessary to consider which mode the DPU is operating in. As Fig. 29 shows, the mode control system generates a two-bit mode control code, R_1R_0, which is the mode number 1, 2, or 3 in binary. The four bits discussed in the previous section plus these two make up the MRD index, $XOP_1P_0R_1R_000$, to which the MRD instruction adds its two-bit address field, W_1W_0 (see Fig. 36) to get the absolute address of the particular file constant it needs.

A specific example is shown in Fig. 37. The CPU is processing a job calling file 1 and the DPU is in mode 2. The MRD index is therefore X 0 0 1 1 0 0 0. The program is executing the MRD instruction to fetch FFM so W_1W_0 = 1 1 and the absolute address becomes X0011011.

Priority System

The priority system accepts job requests, called interrupts, from ten different sources within the DPU. Although these job requests are called interrupts, they are not interrupts in the strict computer sense because they do not interrupt the current job in the CPU. The priority system determines the priority of the jobs in the queue; when the current job is complete, the system passes the highest priority job along with its starting point vector to the CPU. The priority system functions are in the top half of the flow chart in Fig. 31 and in the very top part of Fig. 34. The interrupts, in priority order, are listed in Table 8.

Mode Control

The NAVPAC CPU operates in three major modes. In each mode the data rates from various data sources are different; therefore, the buffer memory must be reallocated for each mode so that the data files all fill at about the same time. As it was described previously, the mode control logic must contribute a two-bit code to the MRD index to control the access of the CPU to the correct set of file constants stored in ROM.

Mode changes are made under command control. Whenever a command is received to change modes, the mode control cycles through a mode-change sequence. First, the mode control initiates

Table 8
Priority Order of Interrupts

Priority	Interrupt
1	Bootstrap loader
2	Dump
3	Receiver time
4	Accelerometer time
5	Telemetry time
6	Accelerometer data
7	Telemetry data
8	Doppler data from receiver 1
9	Doppler data from receiver 2
10	Doppler data from receiver 3

a dump sequence, even though none of the files is full, to empty the memory so that it can be reallocated. Then the mode control sets the bootstrap-loader interrupt. The bootstrap loader is a program that is executed any time that power is first applied to the DPU, or whenever the mode changes to load the complete set of the file constants from ROM into the table of contents. Only when all this has been done is the mode change complete.

Another function of the mode control is to generate masks. Associated with each interrupt (except the first) in Table 8 is a mask or disable function. The mode control senses the command state of NAVPAC and masks out the interrupts associated with any data source that may have been commanded off. For instance, if receiver 1 has been turned off the mode control sets the mask for interrupt 8 and the priority system will no longer respond to any signals (e.g., noise) on that interrupt line.

Input Data Registers

Figure 38a shows that the input data registers consist of a pair of "ping-pong" registers, a parity generator, and associated logic. This connection of registers makes it possible for one register always to output data to the memory while the other one is available to accept data from the input serial data multiplexer. The logic-state diagram is given in Fig. 38b.

Output Data Registers

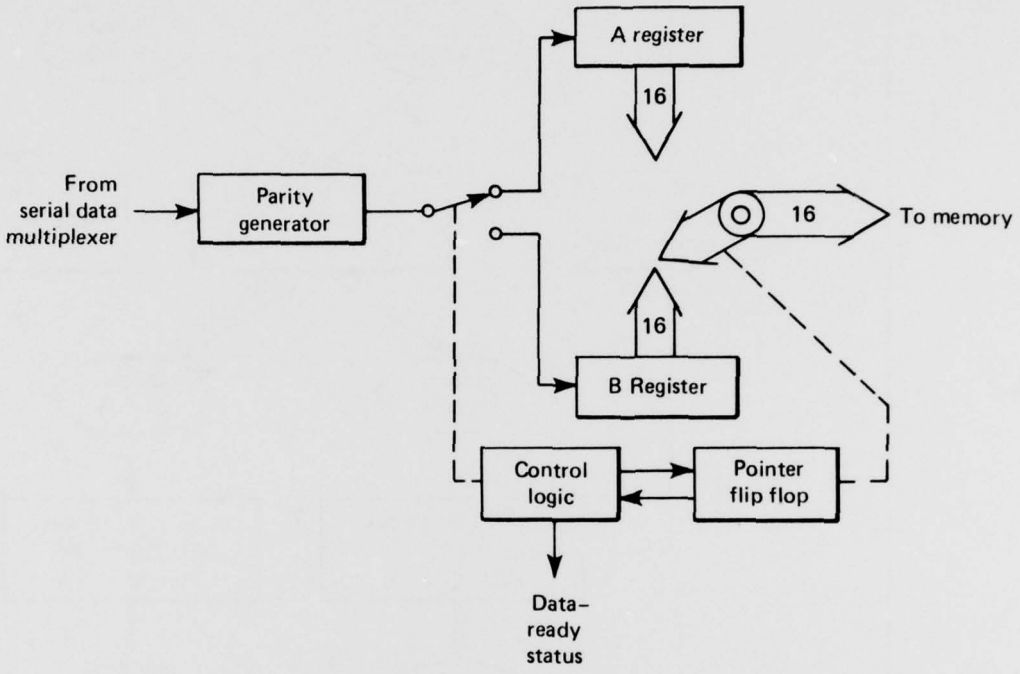
Figure 39a shows that the output data registers are quite similar in nature and construction to the input data registers. During the memory dumping process, one of these registers always outputs to the formatter and tape recorder controller while the other one is being loaded from the memory. The logic-state diagram is given in Fig. 39b.

DATA FORMATTER AND TAPE RECORDER CONTROLLER

The data formatter, which accepts a raw serial data stream from the CPU and formats and encodes it for transmission to the Type 35 flight tape recorder or the SGLS flight transmitter, is at the output of the DPU. The tape recorder controller coordinates the activities of the tape recorder with the data formatter while the contents of the core memory buffer are being recorded on the tape. The tape recorder controller also initiates and controls a reproduce sequence whenever the ground data system requests a tape recorder playback over the SGLS data link.

Functional Description of the Data Formatter

The block diagram of the data formatter is given in Fig. 40. The data formatter constructs a frame of data by adding a sync pattern and a status word to each 60-byte block of data received from the CPU. The format of the 1024-bit frame is shown in Fig. 41. The sync pattern is 11111010111100110010000O (or FAF320 in hexadecimal). The format of the status word is given in Fig. 42. When the CPU does not output data, such as when the tape recorder is coming up to speed, the data formatter fills the data field of each frame with checkerboard (alternating ones and zeros). As shown in Fig. 34, the fifth bit of the status word is cleared to a zero at these times.



(a) Block Diagram

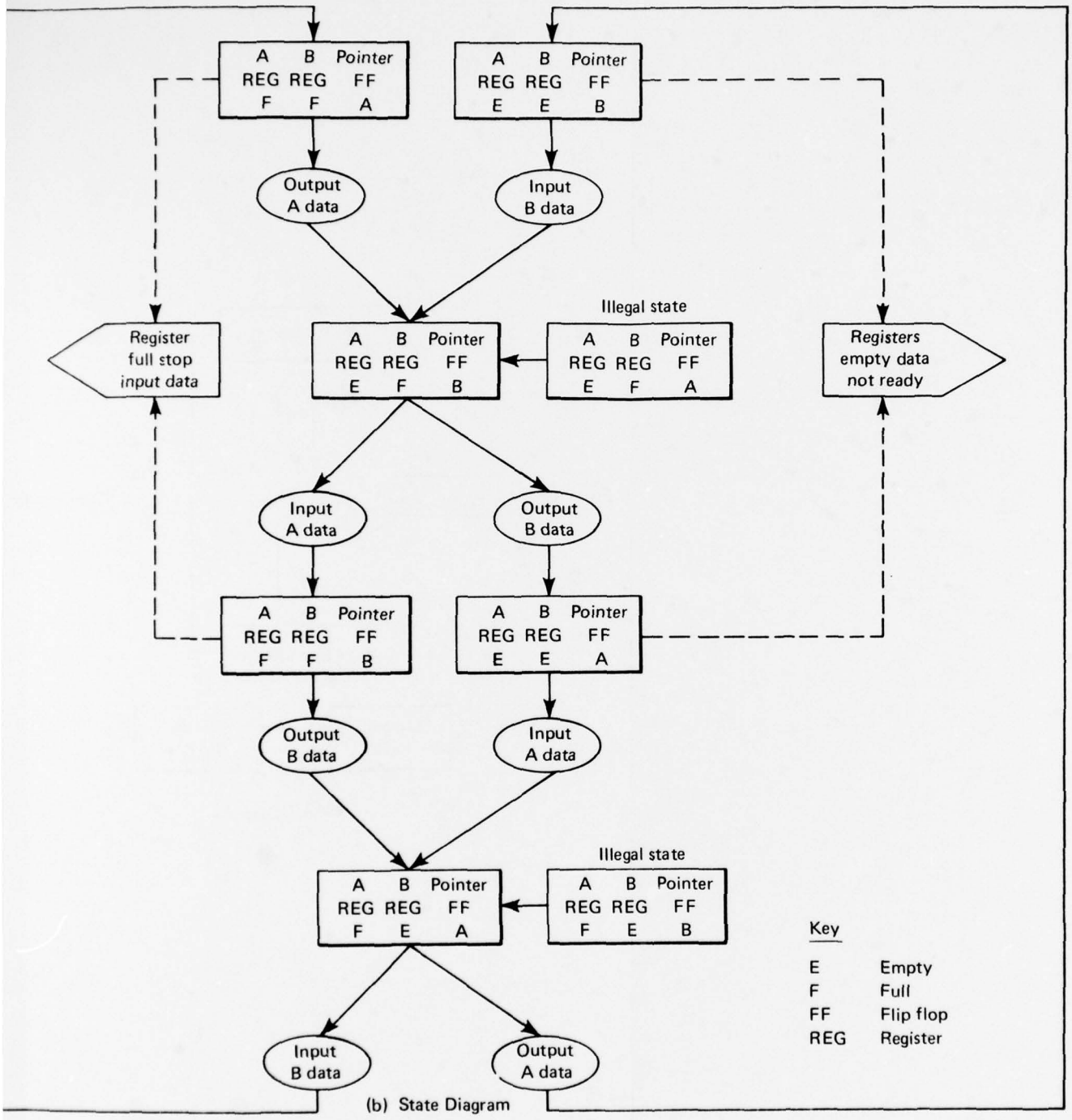
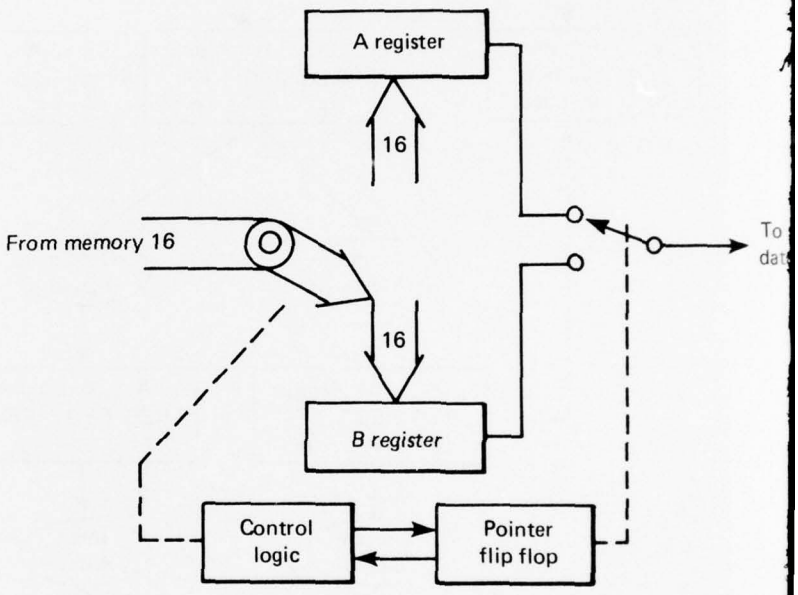


Fig. 38 Input Data Registers



(a) Block Diagram

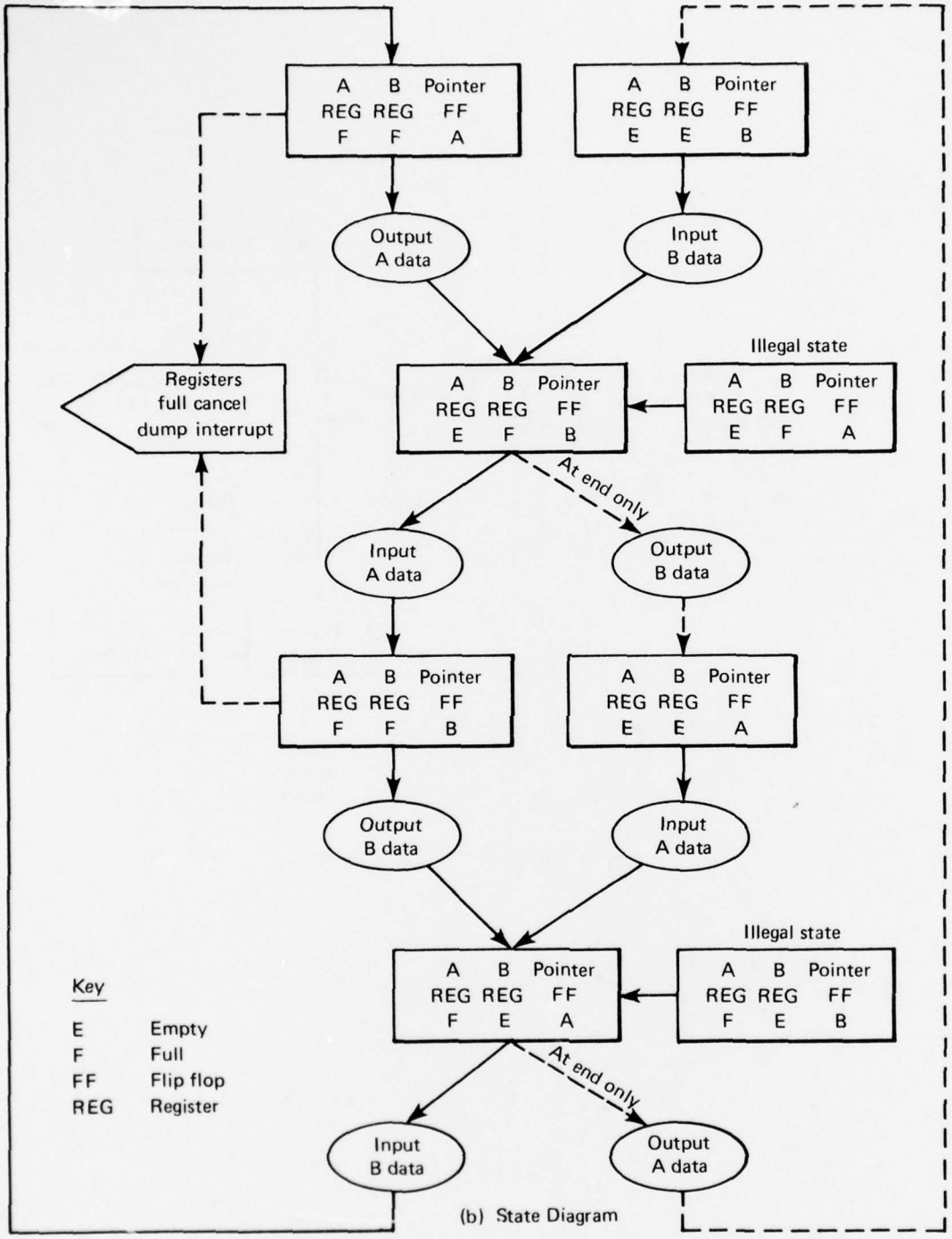
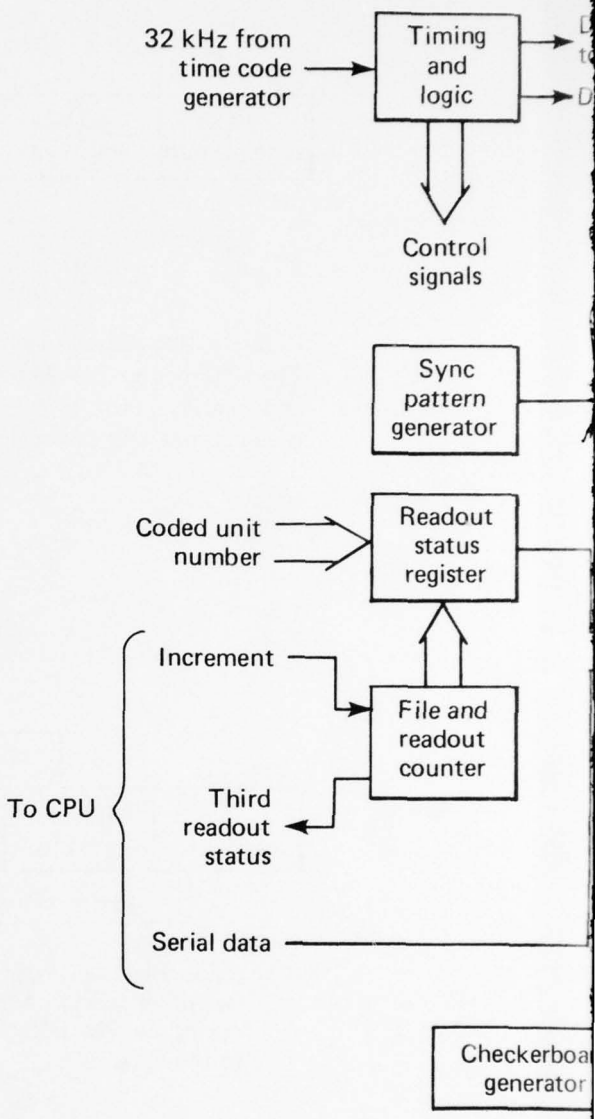


Fig. 39 Output Data Registers

THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
LAUREL, MARYLAND



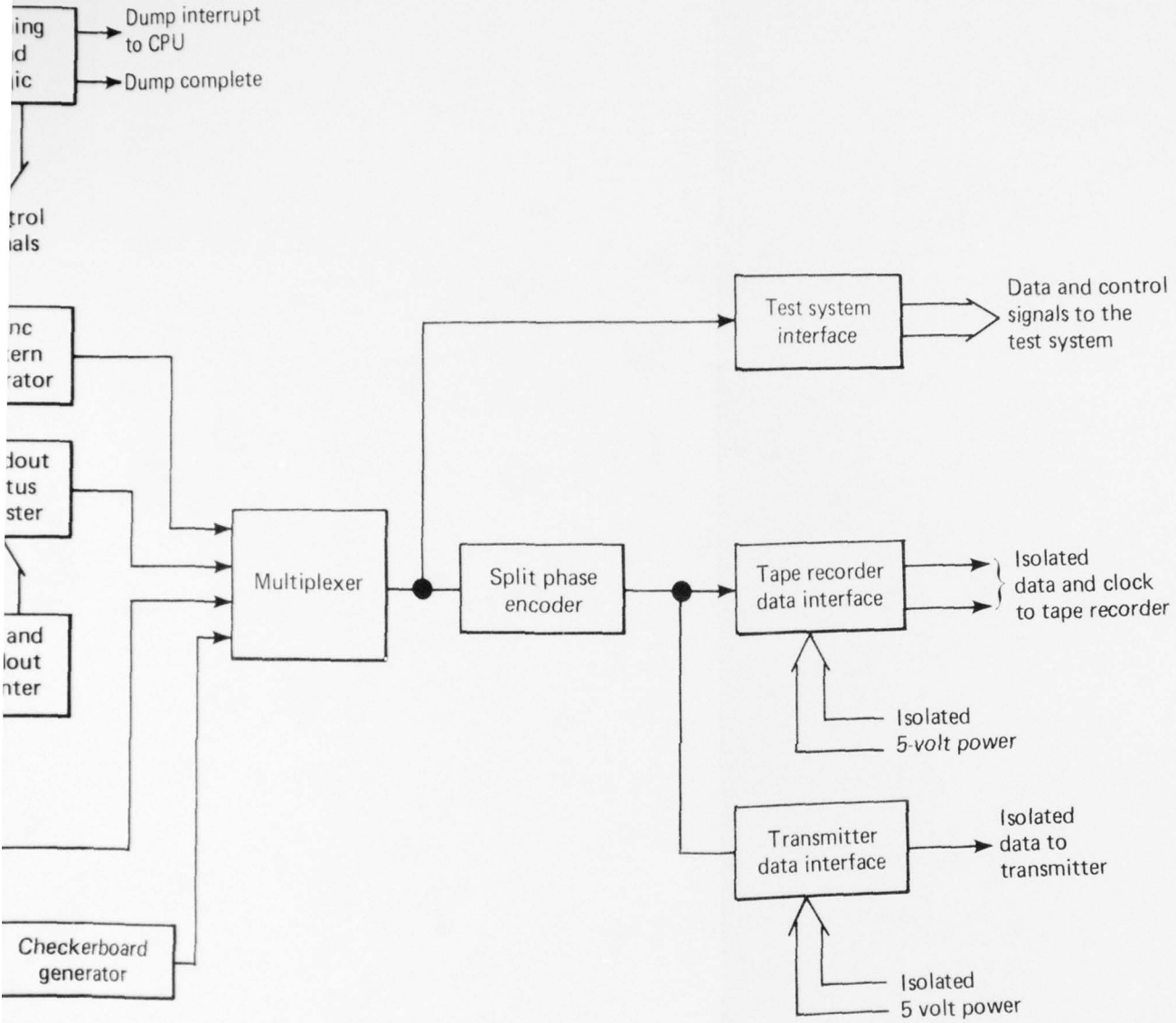
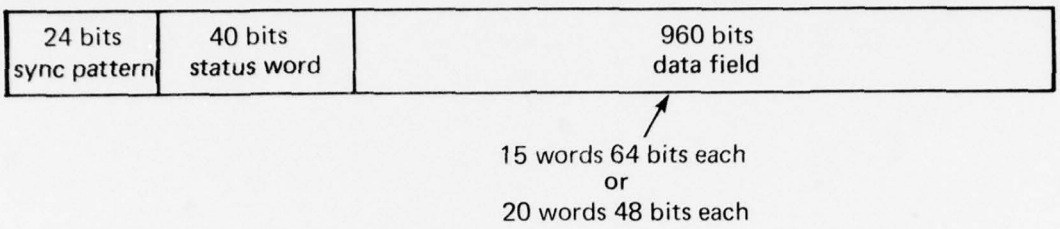


Fig. 40 Block Diagram of the Data Formatter



Data are read out by placing them in a 1024-bit frame. These frames are placed on the Type-35 tape recorder end to end; that is, there are no bits between the end of one frame and the beginning of the next.

Fig. 41 Format of the 1024-Bit Frame

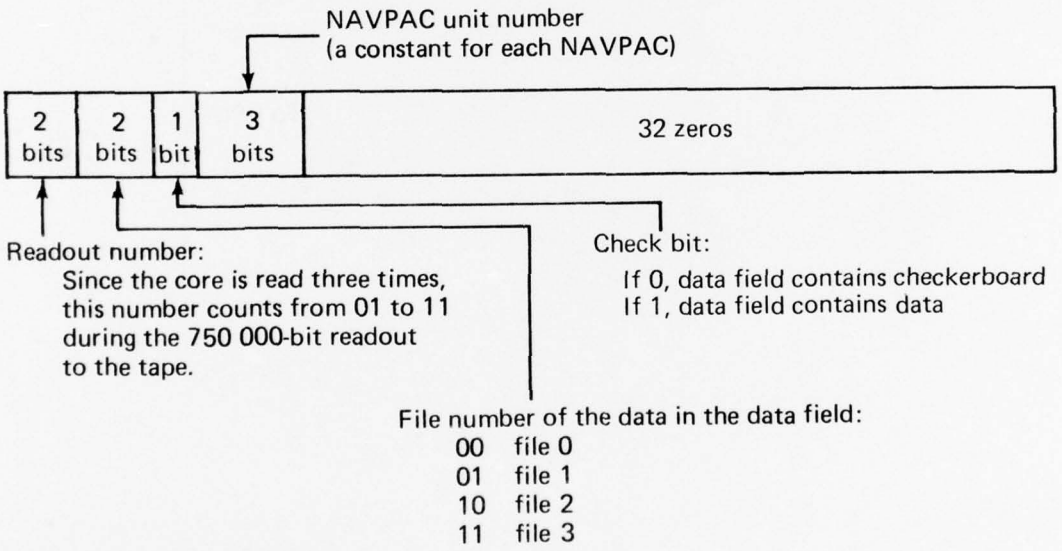


Fig. 42 Format of the Status Word

The data are split-phase (Manchester) encoded. Separately isolated outputs are provided for the tape recorder and the pallet transmitter. The isolation is achieved by optical isolators. Separate outputs, which are neither encoded nor isolated, and special functions are also provided to the test system.

Functional Description of the Tape Recorder Controller

The block diagram of the tape recorder controller is given in Fig. 43. The flow chart for this equipment is shown in Figs. 44 and 45. The following important points should be noted:

1. If the tape recorder is disabled and the buffer memory fills, a hold is generated that masks all the interrupts to the CPU. Nothing further will happen until the transmitter is turned on (to read out the buffer directly to the ground) or a mode change command is sent.

2. Three things will initiate a readout sequence:

   a. The buffer fills and the tape recorder is enabled, or

   b. The transmitter turns on, or

   c. The mode changes.

3. If the transmitter is off, the sequence will end 2 seconds after the third readout of the buffer memory is complete.

4. If the transmitter is on, the sequence will continue to record checkerboard data for 18 seconds after the third readout of the buffer memory is complete, and will then turn off the tape recorder. Four seconds later the tape recorder is directed to play back.

The form of the resulting record on the tape is shown in Fig. 46. The buffer memory fills about once each orbit and the data formatter and tape recorder controller write out one such record. Once a day, over a ground station, the transmitter is turned on to transmit the recorded data back to the ground. This initiates a readout sequence that includes 18 seconds of trailing checkerboard. During playback, the tape direction is reversed and the tape speed is increased by a factor of eight (the playback bit rate is 128 000 bits per second). The tape recorder shuts off automatically when the beginning of the tape is reached.

Detailed Description of the Data Format

When the tape recorder controller turns the tape recorder on, the data formatter begins to output 12 seconds of leading checkerboard. The checkerboard pattern is imbedded in 1024-bit frames in the same manner as the data (see Fig. 41). Each frame begins with sync (FAF320 in hexadecimal). The first four bits of the status word are 0100, meaning that this is the first readout of file 0 (the table of contents). The fifth bit is a 0 meaning that this frame contains only checkerboard. The sixth through the eighth bits are the NAVPAC unit number (refer to Fig. 42). This number is 000 through 101 for Systems 01 through 06.

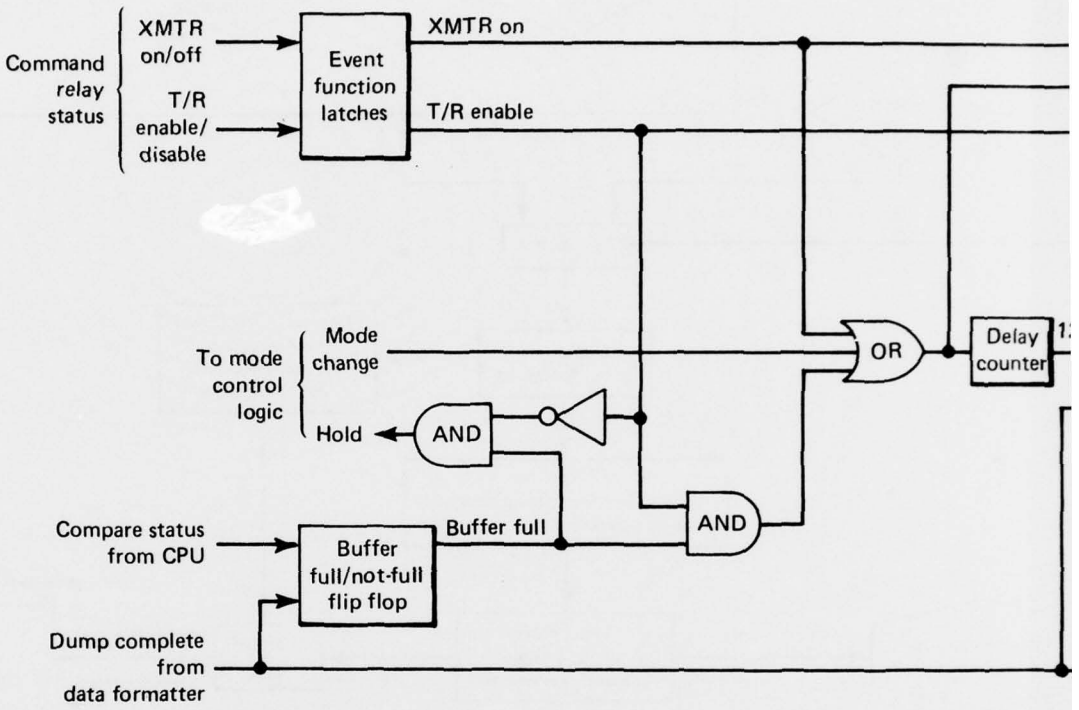
Let us assume this unit is System 01. Then for the leading checkerboard the status word will be 4000000000 (in hexadecimal). This will be followed by 960 bits of checkerboard, which is 240 5's in hexadecimal. This same checkerboard frame will be read out at about 16 frames per second for 12 seconds. Then the status word will become 4800000000 for one frame. The data field for this frame will contain eight 16-bit words of the table of contents followed by checkerboard (208 5's in hexadecimal). Then the status word will become 5800000000 for as many frames as are required to read out the Doppler data (file 1). The last frame will be completed with checkerboard when the data run out. Then the status word will become 6800000000 for as many frames as are required to read out the MESA data (file 2). Then the status word will become 7800000000 to read out the telemetry data. This completes the first readout of the buffer memory.

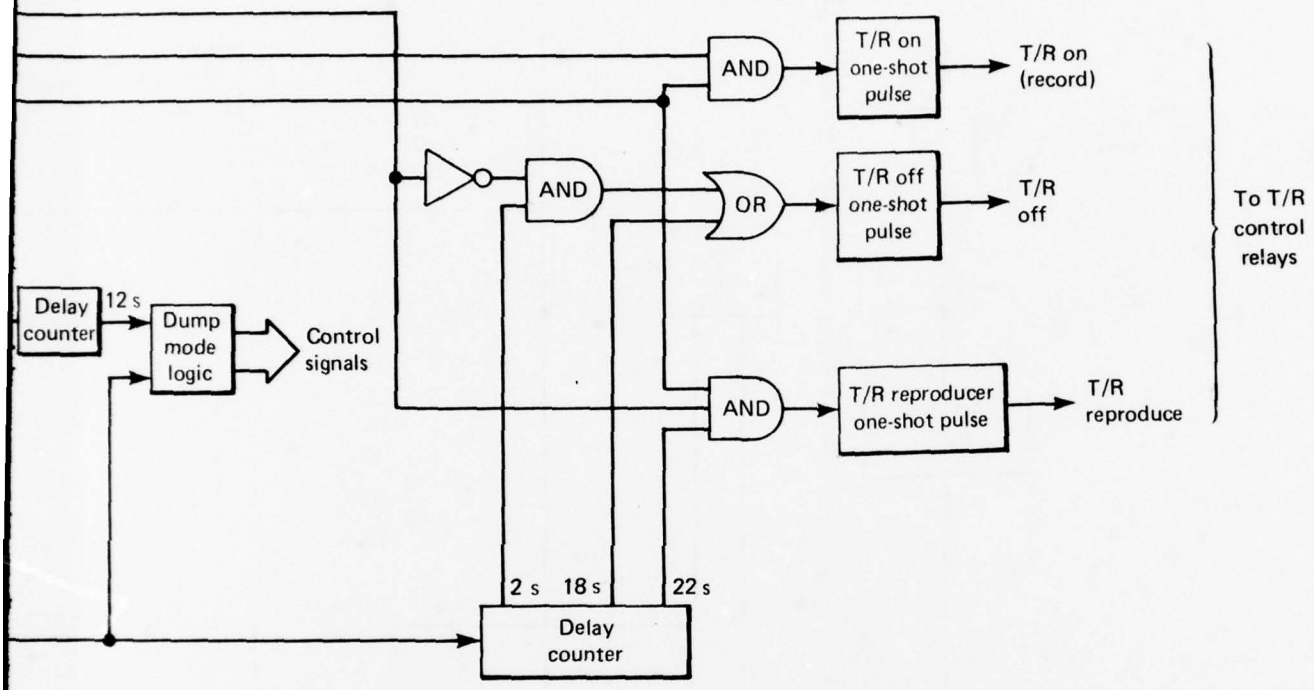
During the second readout the status word begins with 88, 98, A8, and B8 for the table of contents, Doppler data, MESA data, and telemetry data, respectively. This readout includes any new data collected since the first readout took place. The data in the table of contents will of course reflect those new data.

During the third readout the status words begin with C8, D8, E8, and F8. Then during the trailing checkerboard the status word is all zeros.

DOPPLER AND REFRACTION COUNTERS

The DPU contains three Doppler and refraction counters (DRC's). They are labeled DRC1, DRC2, and DRC3 and are connected to the outputs of receivers 1, 2, and 3, respectively. The function of each DRC is to count the uncorrected Doppler frequency and the refraction frequency over accurately controlled 30-second

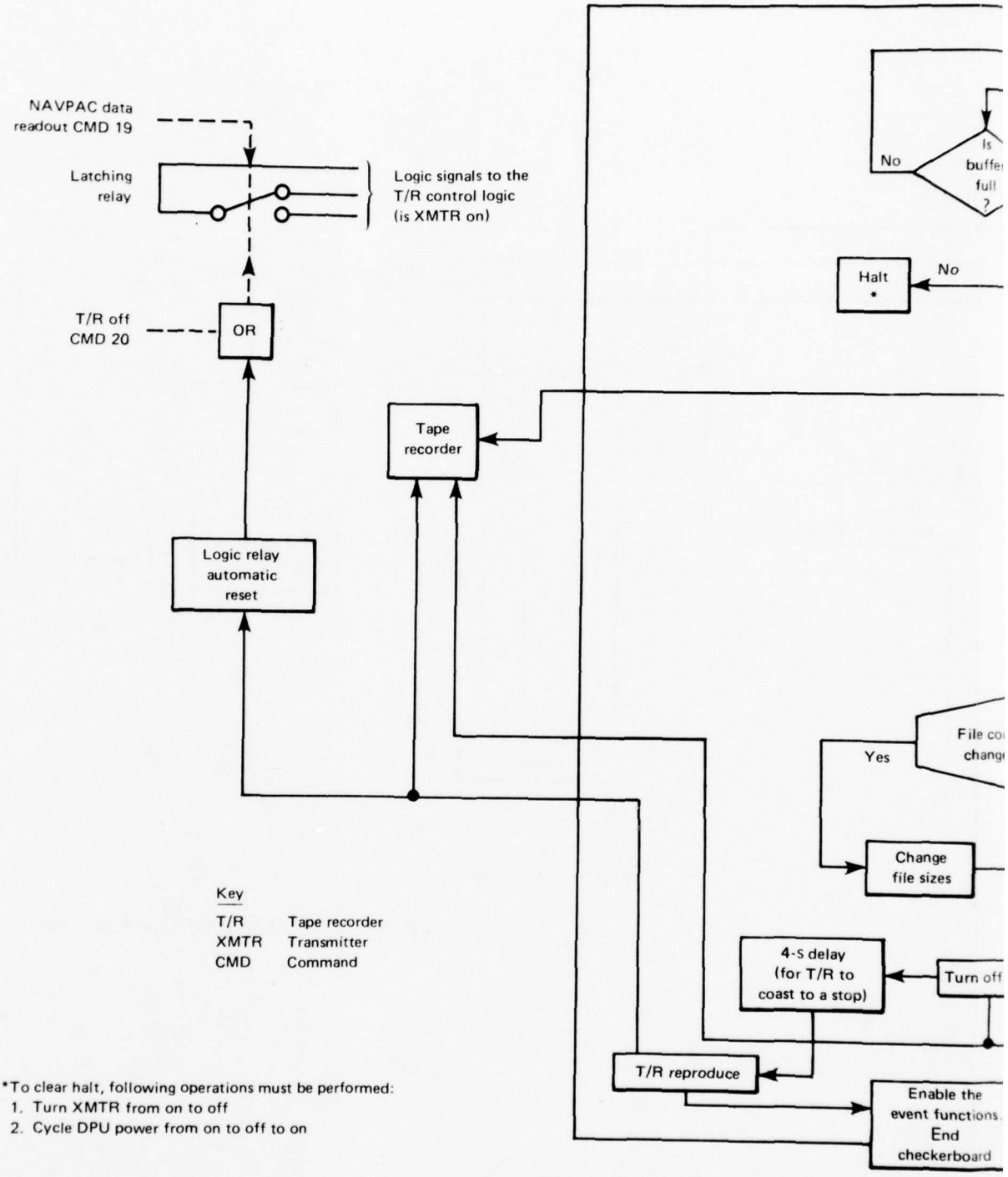

Command relay status
XMTR on/off
T/R enable/ disable
Event function latches
XMTR on
T/R enable
To mode control logic
Mode change
Hold
AND
OR
Delay counter
Compare status from CPU
Buffer full/not-full flip flop
Buffer full
AND
Dump complete from data formatter



Key

T/R Tape recorder
XMTR Transmitter

Fig. 43 Block Diagram of the Tape Recorder Controller



Key

T/R	Tape recorder
XMTR	Transmitter
CMD	Command

*To clear halt, following operations must be performed:
1. Turn XMTR from on to off
2. Cycle DPU power from on to off to on

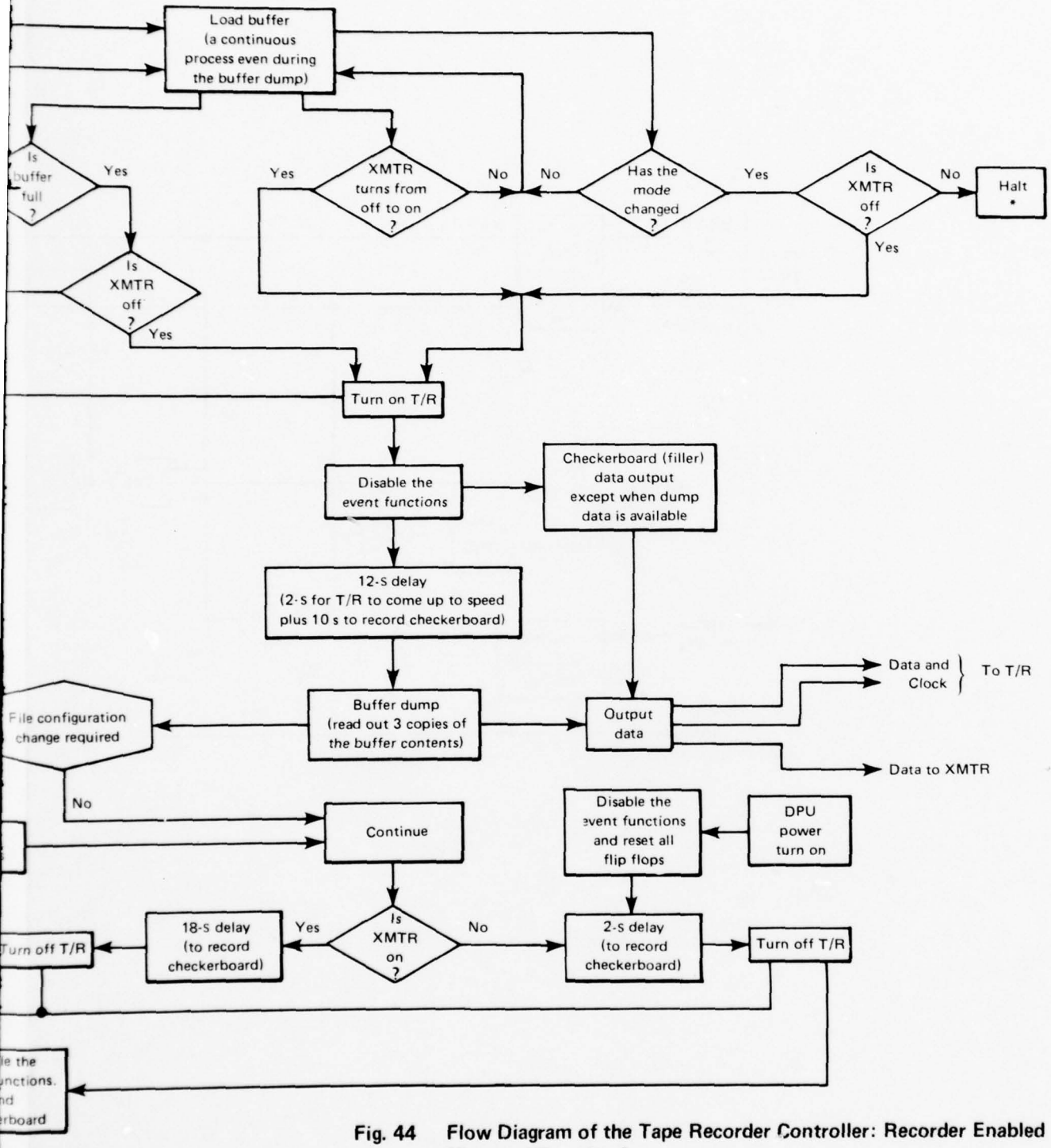
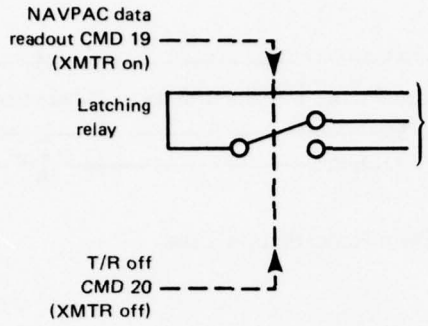
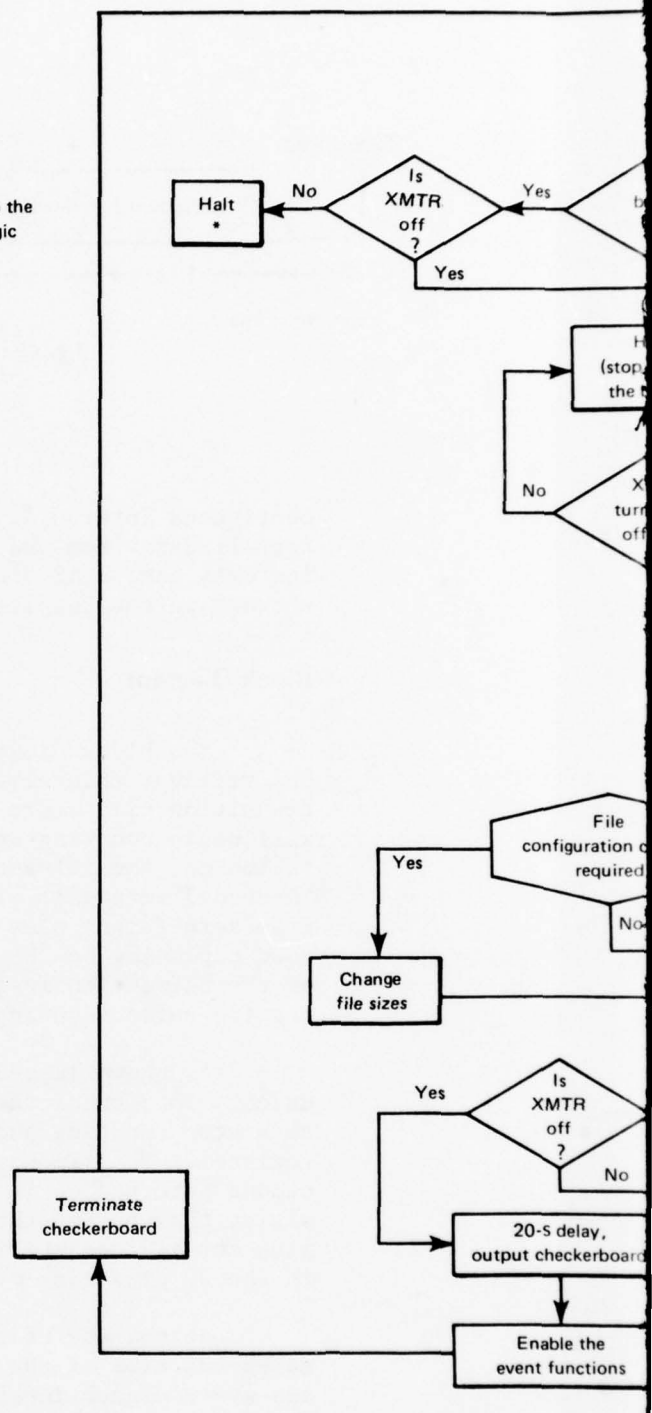


Fig. 44 Flow Diagram of the Tape Recorder Controller: Recorder Enabled (System 02, and up)





Key

T/R	Tape recorder
XMTR	Transmitter
CMD	Command

*To clear halt, following operations must be performed:
1. Turn XMTR from on to off
2. Cycle DPU power from on to off to on

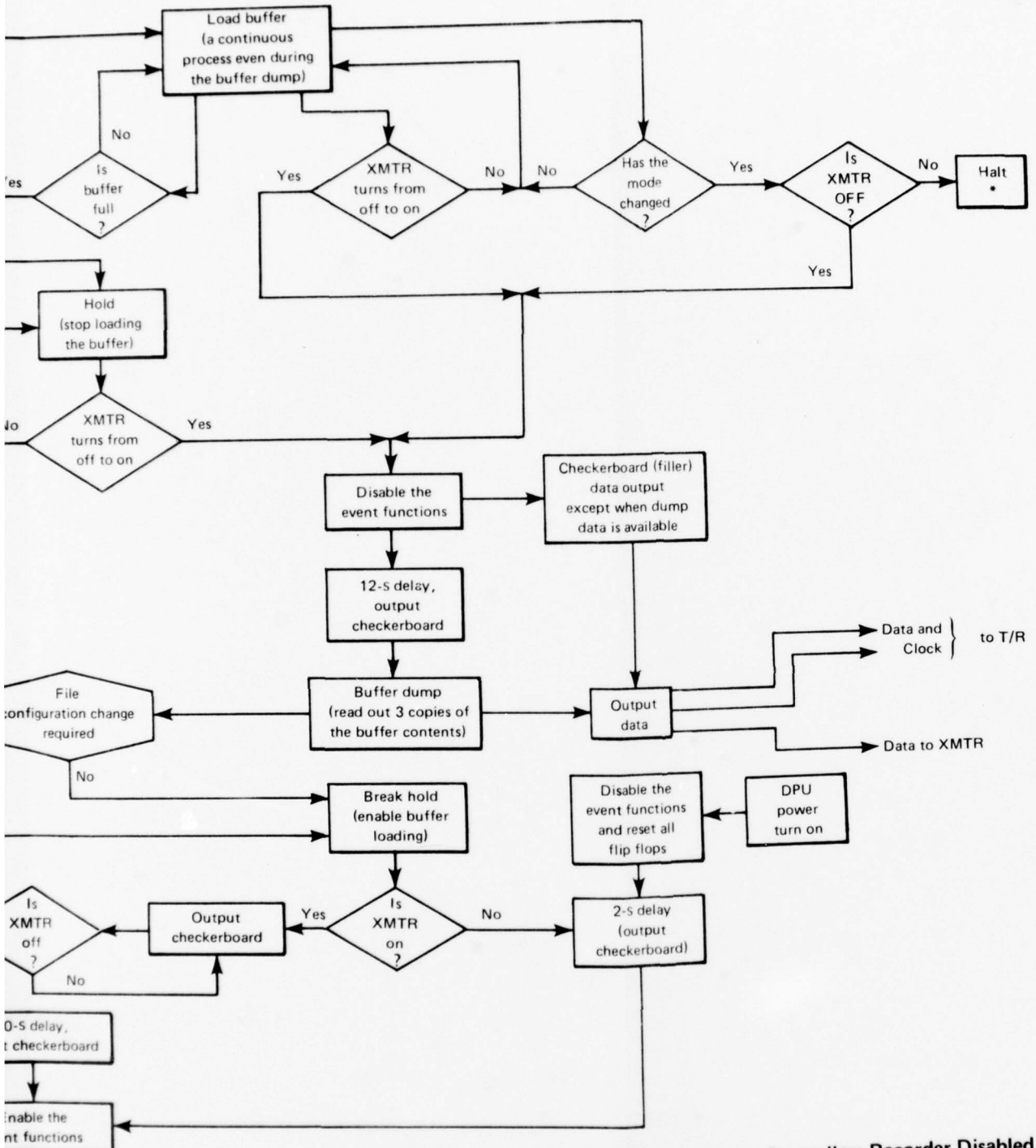


Fig. 45 Flow Diagram of the Tape Recorder Controller: Recorder Disabled (System 02, and up)

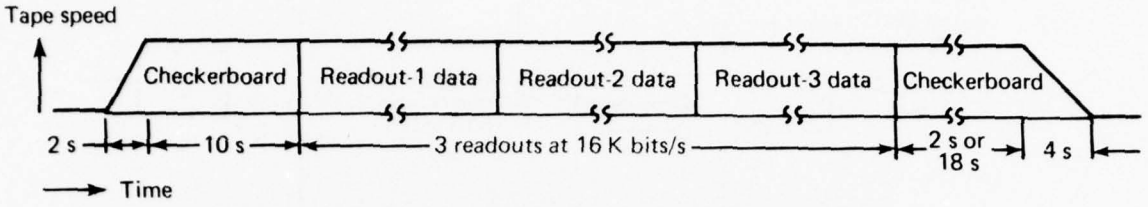


Fig. 46 Form of the Data Recorded on Tape

contiguous intervals. The DRC must request proper time annotation for all data from the time code generator (TCG). The DRC formats its data into a 48-bit word, which it passes along to the CPU for storage in the Doppler data file.

Block Diagram

The block diagram of a DRC is shown in Fig. 47. If the 400-MHz receiver channel is locked, the very first negative-going zero transition will start the 30-second gate and the Doppler counter will begin counting up from zero. If the 150-MHz receiver channel is locked, the refraction counter will also count during this same 30-second interval. The refraction counter also starts counting from zero (sign, plus twos complement), but it may count up or down depending on the sign of the refraction frequency. The sign of the refraction frequency depends on the phase relationship of the two refraction inputs as shown in Fig. 48.

As shown in the timing diagram (Fig. 47), at the end of exactly 30 seconds the Doppler counter and the refraction counter both stop counting and transfer their contents to the output shift register. The time-over counter now counts from the end of the 30-second interval until the next Doppler negative-going zero transition that begins the next 30-second interval. The Doppler count plus one is then the integral number of Doppler cycles that occurred in the 30 plus time-over count seconds.

At the end of the 30-second interval (see Fig. 48) the TCG marks the time of the first of a series of contiguous intervals and every eighth interval thereafter. Only when the 400-MHz receiver channel drops lock are all intervals prevented from being

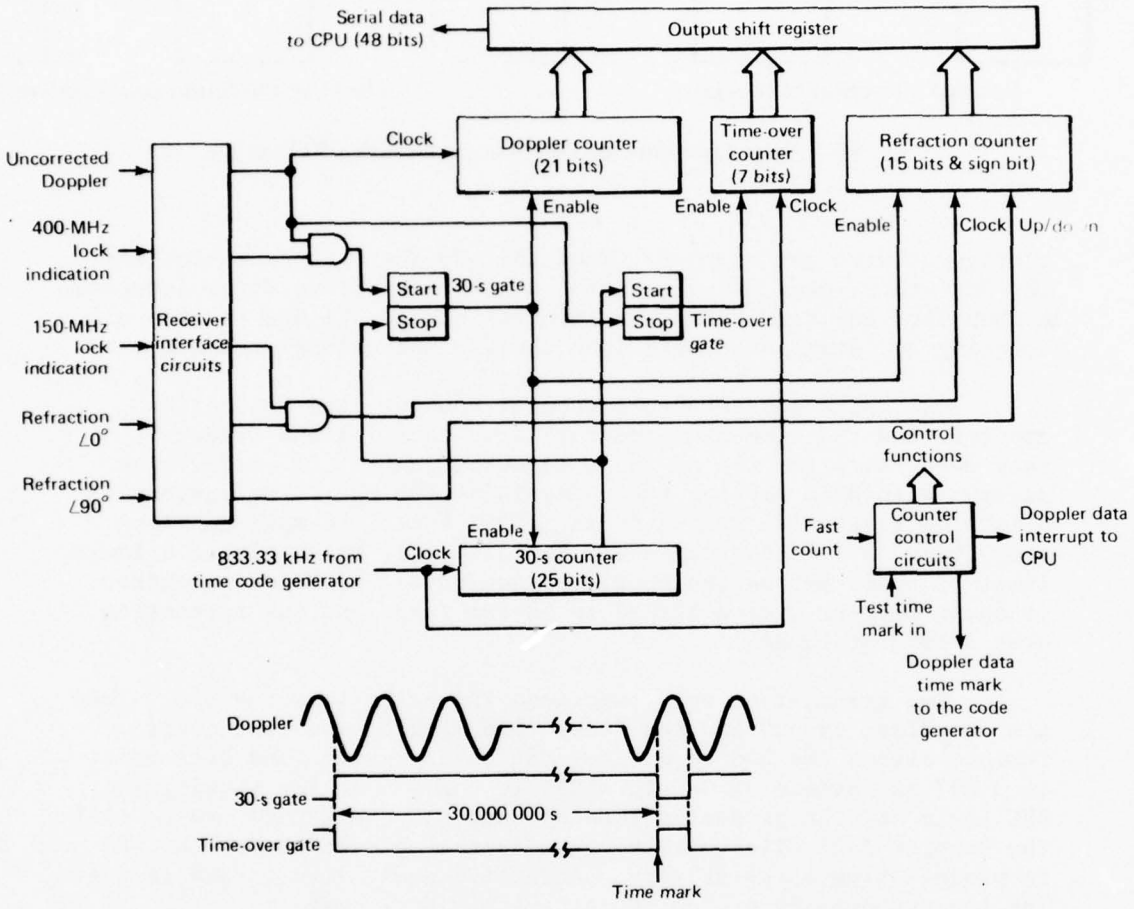


Fig. 47 Functional Block Diagram of One NAVPAC Doppler and Refraction Counter

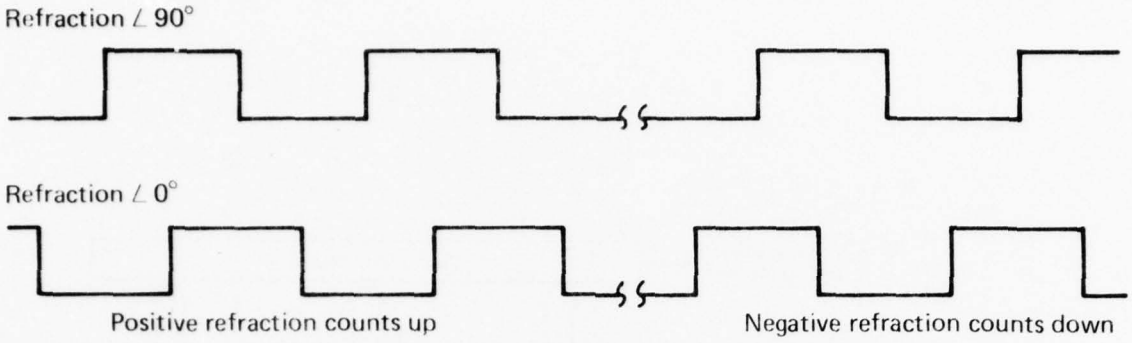


Fig. 48 Phase Relations for Positive and Negative Refraction

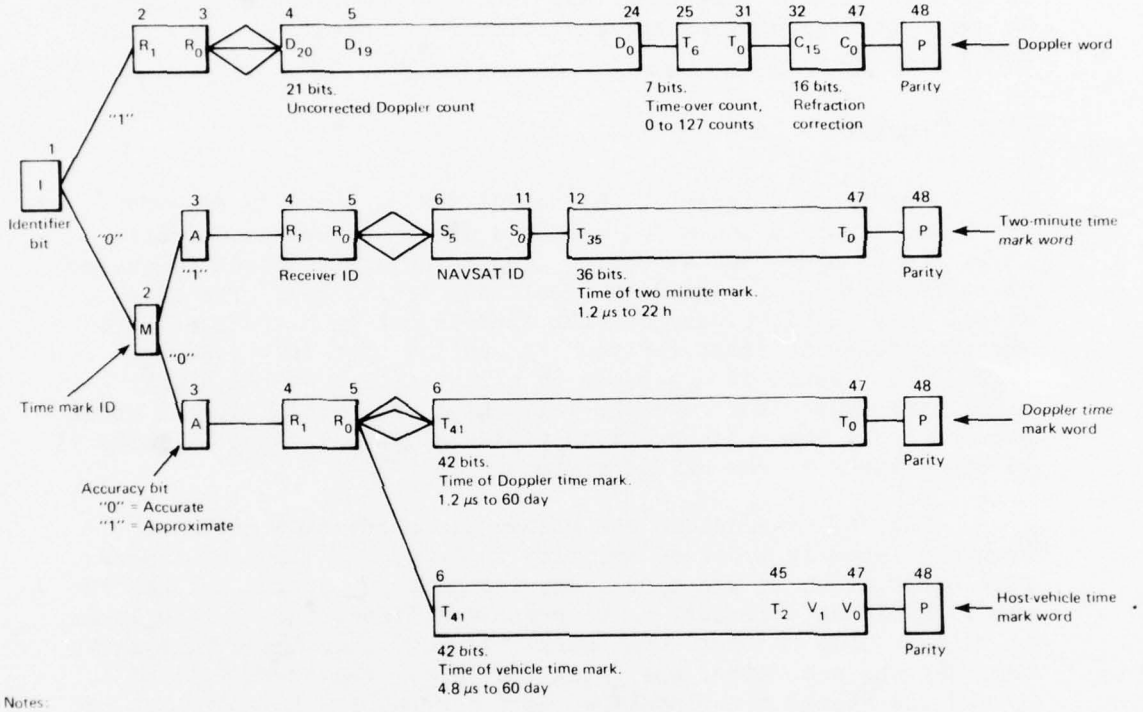
contiguous with one another. When the 400-MHz channel reacquires, the DRC starts over and marks time at the end of the first interval. A drop lock any time during an interval causes the DRC to stop all counting and start over only when the 400-MHz channel reacquires.

All three counters (the Doppler counter, the refraction counter, and the time-over counter) stop counting and freeze if they ever reach the top of their counting range (all ones). The maximum allowable Doppler frequency is 69.905 kHz. The maximum allowable refraction frequency is ±1.092 kHz. The maximum time-over count is 127 (corresponding to 152.4 μs), which places a lower limit of 6.562 kHz on the Doppler frequency. The DRC is required to count Doppler over a 12-kHz to 52-kHz range and the refraction over a ±600-Hz range.

Two ground-test-only functions are built into the DRC. They are the "fast count" and the "test time mark." The fast count feature allows the DRC to collect data much faster (one data point in 3.697 ms instead of 30 s). This is convenient for testing the DRC logic and for producing lots of data for the CPU to use to fill the Doppler data file quickly. The test time mark allows the DRC to produce time marks at very accurately known times to aid in testing the performance of the TCG at system level test.

Data Format

The format of the 48-bit data word generated by the DRC is shown at the top of Fig. 49.



Notes:

1.

	R_1	R_0
Host vehicle	0	0
Receiver 1	0	1
Receiver 2	1	0
Receiver 3	1	1

2. Odd parity is generated in the central processor; i.e., the number of "ones" in each word is constrained to be odd.

3.

	V_1	V_0
Host-vehicle time 0	0	0
Host-vehicle time 1	0	1
Host-vehicle time 2	1	0

Fig. 49 Format of the 48-Bit Data Word

TIME CODE GENERATOR

The timekeeping element of the DPU is the TCG. It accepts a very accurate, very stable 5-MHz signal from the NAVPAC oscillator and keeps time and provides timing signals for the DPU and the rest of the NAVPAC system. The TCG marks time of occurrence of eleven different events, formats time words representing these events, and passes the words to the CPU for storage in the proper data files. The TCG keeps time with a resolution of 1.2 μs for up to 60 days without repeating (provided the power is not turned off). It can handle as many as three simultaneous (within 1.2 μs) time marks without error.

Block Diagram

The block diagram of the NAVPAC TCG is shown in Fig. 50. The 5-MHz input is converted from a 0 dBm sine wave to a square wave, and then divided by six to create the master clock frequency of 833.33 kHz (hence the time resolution of 1.2 μs). The clock itself is a 42-bit binary counter that is set to a count of zero whenever power is first applied. A special test-only feature, called fast count, is available to allow testing of the higher order bits (since the clock normally will only repeat itself after two months). The clock provides timing signals (listed in Table 9) to other parts of the NAVPAC system.

The TCG responds to the eleven different time marks or events, listed in order of priority in Table 10. If two or more time marks occur at the same time, the priority system selects the one with highest priority to be processed first; then 1.2 μs later, it will process the next time mark. If more than three time marks occur at the same time, the three TCG output registers will fill up and the fourth time mark must wait for the CPU to empty one of the output registers. When a time mark must wait to be processed, one bit in the time word flags the condition, alerting the user of the data to the fact that this time data point may not be completely accurate.

The time marks can be masked so that the TCG will not respond to signals (e.g., noise) from a particular equipment that is off or not in use.

The NAVSAT identification, which is recovered from the NAVSAT navigation message by the navigation message recovery unit (NMR), is provided to the TCG to be included as part of the two-minute time-mark word.

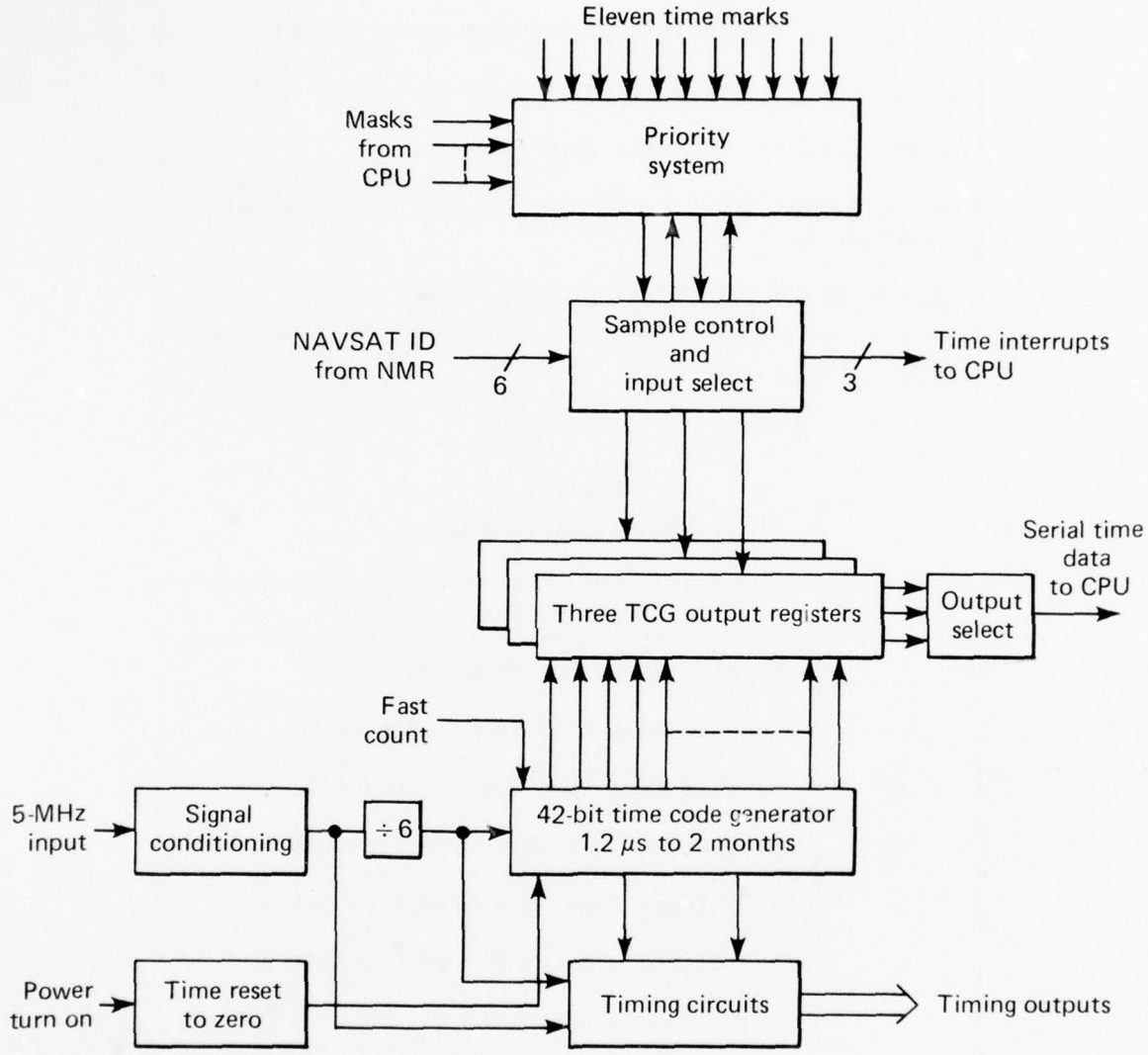


Fig. 50 Functional Block Diagram of the NAVPAC Time Code Generator

Table 9

Timing Outputs from the Time Code Generator

2.5 MHz for the navigation message recovery unit
Six buffered outputs of the 833.33-kHz master clock
32.0512 kHz for the data formatter
One buffered output of 814 Hz for each of the three receivers
25.4 Hz for the receiver priority logic

Table 10

Priority Order of Time Marks

Priority	Time Marks
1	Doppler data time from receiver 1
2	Doppler data time from receiver 2
3	Doppler data time from receiver 3
4	Two-minute time mark from receiver 1
5	Two-minute time mark from receiver 2
6	Two-minute time mark from receiver 3
7	Host-vehicle time mark 0
8	Host-vehicle time mark 1
9	Host-vehicle time mark 2
10	Accelerometer time
11	Telemetry time

The three interrupts from the TCG to the CPU are (a) receiver-time interrupt, which occurs as a result of time marks 1 through 9; (b) acceleromater-time interrupt, which occurs as a result of time mark 10; and (c) telemetry-time interrupt, which occurs as a result of time mark 11.

Time Word Format

The formats of the five different kinds of time words generated by the eleven different time marks are shown in Figs. 49 and 51.

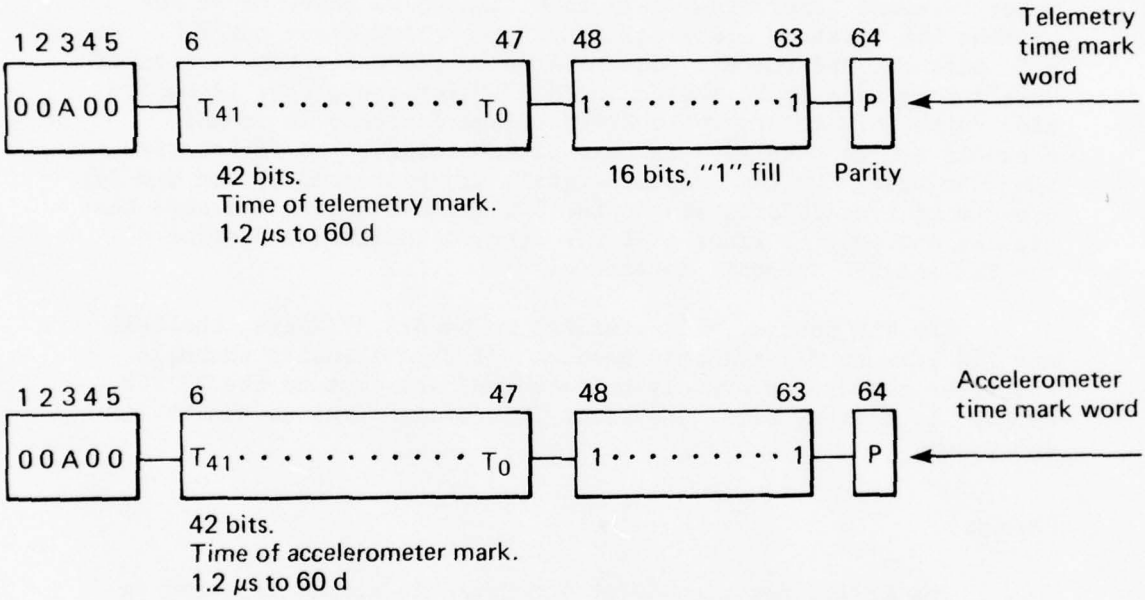


Fig. 51 Format of the NAVPAC Time Word

TELEMETRY

The NAVPAC telemetry (TLM) is a subsystem contained within the DPU. The TLM subsystem samples analog and discrete (telltale) information from the various subsystems and formats the information for readout to the data processor for subsequent transmission to earth. Telemetered information is basically housekeeping, temperatures, and status for monitoring the performance of the NAVPAC.

Other functions performed by the TLM include the processing of MESA data for readout by the DPU, generation of independent analog (10 channels) and discrete (24 bits) information to the HV TLM subsystem, and an interface to process the HV time-marker signals.

Block Diagram

A block diagram of the NAVPAC TLM is shown in Fig. 52. Analog and digital inputs are commutated from the DTL's, DC/DC converter, and the relay package. The internal interface between TLM and the DPU consists of (a) signals that read out the TLM bit stream, (b) signals that read out the MESA bits, and (c) several mode-control signal lines that essentially select either a fast or slow repetition rate of reading out TLM bits to the DPU memory. Other internal interfaces cause time tags to be inserted in the TLM or MESA bit streams. External interfaces exist among the TLM, the MESA package, and the HV. The MESA interface generates 64 bits of MESA information to be stored in the TLM for subsequent transmission to the DPU memory. The HV interface includes 10 analog channels and 24 discrete channels of TLM information for the HV TLM subsystem. HV time marker signals are processed by the TLM for storage of time information in the DPU memory. There are some test signals and control lines that are used to facilitate testing of the TLM and DPU internal interface.

The TLM subsystem is designed to handle 35 analog channels and 112 bits of digital information. Of the 35 analog channels, the first ten are separately buffered and are sent to the HV TLM. Of the 112 digital bits, the first 24 are also sent to the HV TLM subsystem.

Format

The format for the NAVPAC TLM data-bit stream is shown in Fig. 53. Each analog channel consists of an 8-bit digital word that is the result of an 8-bit analog-to-digital conversion of that channel's data. There are seven such analog channels plus an 8-bit identifier word for each subframe. The identifier word is the last word of each subframe to be shifted out to the DPU memory. The identifier word consists of three subframe bits, two frame bits, two "don't care" bits, and a parity bit, which the DPU determines and inserts into the bit stream. Identifier-bit definitions are shown in Fig. 53. There are seven subframes for each TLM frame. There are four frames for each TLM cycle. After each cycle, the TLM subsystem requests a time tag from the TCG to be inserted into the TLM bit stream.

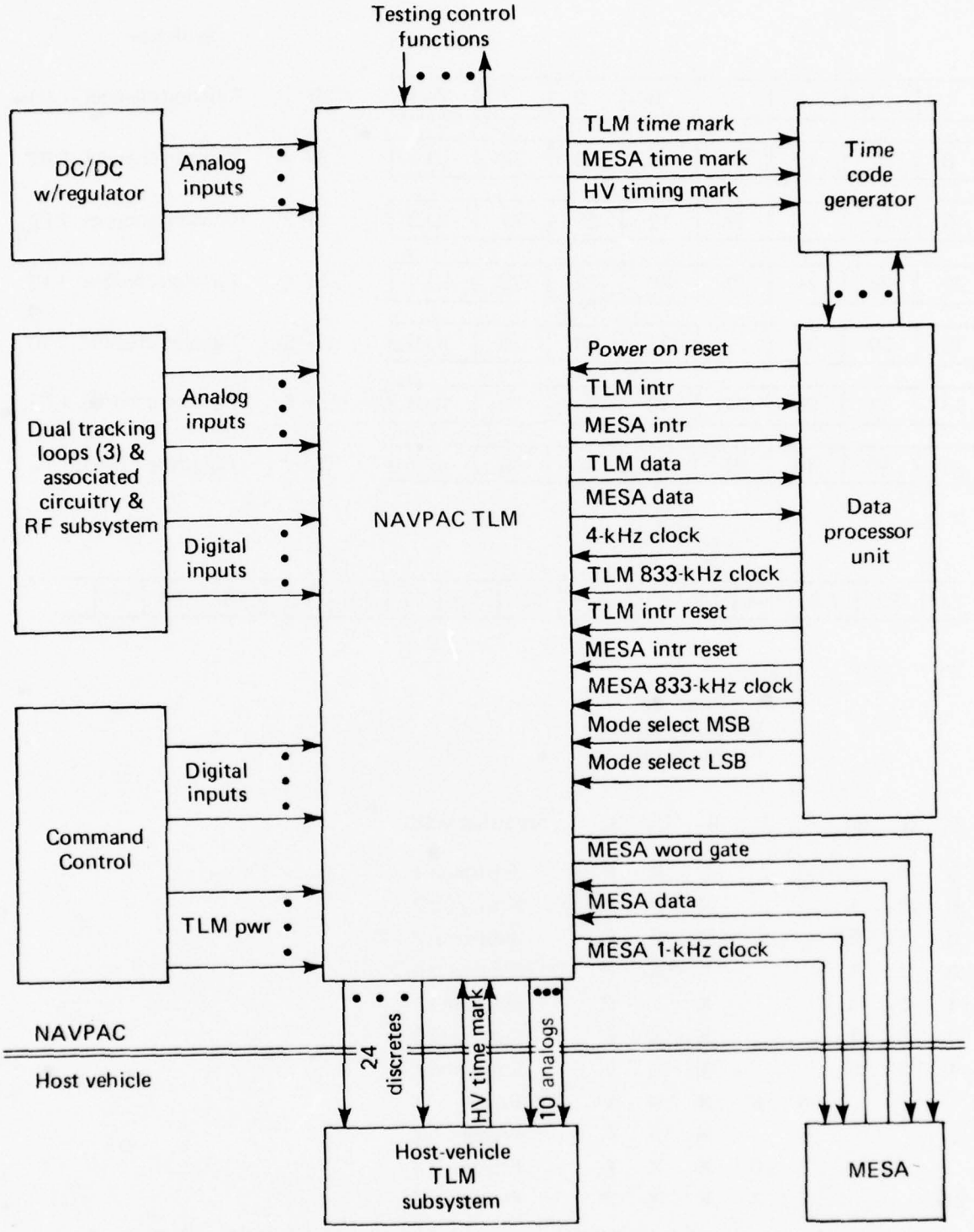


Fig. 52 Block Diagram of the Telemetry Subsystem

								Subframe	
1	2	3	4	5	6	7	ID 1	SF 1	7 analog channel, 1 ID
8	9	10	11	12	13	14	ID 2	SF 2	7 analog channel, 1 ID
15	16	17	18	19	20	21	ID 3	SF 3	7 analog channel, 1 ID
22	23	24	25	26	27	28	ID 4	SF 4	7 analog channel, 1 ID
29	30	31	32	33	34	35	ID 5	SF 5	7 analog channel, 1 ID
36	37	38	39	40	41	42	ID 6	SF 6	7 discrete words, 1 ID
43	44	45	46	47	48	49	ID 7	SF 7	7 discrete words, 1 ID

(a)

F1	F2	F3	F4	TT	F1	F2	F3	F4	TT	F1	F2	F3	F4	TT	...

(b)

Key

TT = *Time tag*
X = Don't-care bits
P = Parity bit

B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	Identifier word
0	0	0			X	X	P	Subframe 1
0	0	1			X	X	P	Subframe 2
0	1	0			X	X	P	Subframe 3
0	1	1			X	X	P	Subframe 4
1	0	0			X	X	P	Subframe 5
1	0	1			X	X	P	Subframe 6
1	1	0			X	X	P	Subframe 7
			0	0	X	X	P	Frame 1
			0	1	X	X	P	Frame 2
			1	0	X	X	P	Frame 3
			1	1	X	X	P	Frame 4

(c)

Fig. 53 Format of the Telemetry Data-Bit Stream: (a) Telemetry Frame, (b) Telemetry Cycle, and (c) Identifier-Bit Definition

There are two readout modes for the TLM bit stream. The slow mode causes interrupts to the DPU to be generated by the TLM for readout of each subframe of information (64 bits) once every 16 seconds. The fast mode causes the readout to the DPU once every two seconds. A time tag is inserted in the TLM data stream once every second (fast mode) and once every eight seconds (slow mode) after the seventh TLM interrupt of each fourth TLM frame.

A MESA data sample (64 bits) is accumulated every two seconds. A time tag is inserted in the MESA data stream once every 32 data samples.

NAVPAC MESSAGE RECOVERY (NMR) UNIT

General Description

The purpose of the NMR is (a) to establish a clock that runs in phase synchronization with the received modulation from the satellite being tracked, (b) to recognize the two-minute mark and send a signal to the processor, and (c) to extract the satellite identification number from the data. Signals from three receivers are input to the circuit, but only one signal is sampled at a time.

The cosine of the received phase modulation is used as the input to a phase-locked loop that locks a digital clock to the doublet rate. The sine of the received modulation is converted from an analog to a digital signal and the resulting ones and zeros are decoded for the two-minute time mark and the satellite identification.

Implementation

Receiver Signals. Input signals from each of the three receivers are the sine and cosine of the received phase modulations and a corresponding Doppler-lock signal. A commutator controlled by a divide-by-eight counter is used to sample each receiver, in sequence. The first receiver is sampled on the first clock pulse after the counter is reset and each successive clock pulse advances the commutator to sample a different receiver. The fourth clock pulse resets the counter and the cycle begins again with the first receiver.

A flip-flop is set when a receiver with a true Doppler-lock signal is sampled. The output of the flip-flop is the clock inhibit input of the commutator counter, allowing the receiver with the

Doppler-lock signal to remain sampled until the flip-flop is reset, and preventing the commutator from advancing to the next receiver. Other uses of the output are to turn on a switch that allows the cosine of the received phase modulation to pass to the phase-locked loop and to enable the clock of a timer that resets the flip-flop after a certain period of time.

The flip-flop is reset in one of four ways. First, when the circuit is initially powered, an RC circuit provides a signal that resets the flip-flop. After this, the flip-flop reset will depend on the satellite signal received. If doublet correlation has not been achieved within 30 seconds, the flip-flop is reset and the phase-locked loop will not continue to sample the cosine signal. However, if doublet correlation is achieved, the flip-flop will not reset until the time mark has been decoded and a signal has been sent to the processor. In any case, the flip-flop is reset after four minutes, even if no two-minute time mark has been decoded prior to that time.

Once the flip-flop is reset, the commutator continues to cycle until a receiver that has a true Doppler-lock signal is sampled. The sine and cosine signals are again sampled until the flip-flop is reset.

Doublet Rate Clock. The clock (Ref. 1, Vol I, pp. 4-28, 4-29) is generated by a two-order phase-tracking loop. The loop is first-order in the acquisition mode and it is second-order while in the track mode. The loop is composed of a frequency divider, a phase comparator, a loop filter, an analog-to-digital pulse-rate converter, and pulse add-delete circuits. The output is the doublet rate clock, running at the doublet rate.

The frequency divider is a digital counter that divides a 2.5-MHz signal (derived from the NAVPAC reference oscillator) by 24 576. To each period of the resulting waveform, 0.8 μs is added to generate an effective division ratio of 24 578. The resultant nominal frequency is 101.716983 Hz with a period of 9831.2 μs. The nominal doublet period transmitted from the satellite is 9831.2305 μs. The period change due to Doppler can be as high as ±20 ppm or ±0.2 μs/doublet.

The phase comparator is a full-wave quadrature chopper and an amplifier that detects the phase difference between the cosine input signal and the derived doublet clock, and provides complementary DC error voltages to the loop filter.

Ref. 1. "Doppler Receiving Set, Portable Precision Differential (DRS/PPD)," Vols. 1 and II, Honeywell.

The loop filter is a two-order switchable circuit. It contains an operational amplifier configured as a damped integrator or amplifier (depending on whether the loop is in the track or acquisition mode). The DC voltage from the loop filter is proportional to the phase error between the cosine phase input and the doublet rate out. The mode of operation of the loop filter depends on the state of a switch across the integrating capacitor. During the acquisition phase, the absence of a doublet correlation signal allows the switch to short out the integrating capacitor so that the loop filter is a straight amplifier. Once doublet correlation is achieved, the short is removed and the loop filter becomes an integrator. The loop is then configured as a second-order loop.

The analog-to-pulse-rate converter is a bistable feedback loop that is clocked at 8 times the doublet rate or 32 times the doublet rate (depending on whether the loop is in the track or acquisition mode). The clocking rate has the effect of changing the gain of the converter. The output state of the converter determines whether 0.8-μs time increments are to be added or deleted from the nominal derived doublet period.

The add-delete circuits provide the fine adjustment of the doublet clock. The combination of the add-delete circuits, the analog-to-pulse-rate converter, and the counter is analogous to a VCO with a scale factor of 0.00072 Hz/V.

Doublet Correlation (Ref. 1, Vol. I, p. 4–22). The cosine output is cross-correlated with the doublet rate timing signal and filtered with a 1-Hz low-pass filter, resulting in a DC voltage that is proportional to the percentage of phase lock. Doublet lock is indicated when the correlation voltage is greater than 0.38 V. When the correlation voltage drops below 0.13 V, the lock indicator is reset, indicating loss of lock.

Once doublet correlation is achieved, the loop becomes second-order. Doublet correlation also enables the counter used during bit synchronization and prevents the input commutator from advancing after 30 seconds. Without doublet correlation, the circuit will not process the sine signal and the commutator will resume its cycle.

Data Decoder (Ref. 2, pp. 6.26 through 6.28). The sine of the received modulation contains the ones and zeros that make up the satellite

---

Ref. 2. "MX706 Satellite Navigation System: Operation and Maintenance Manual," The Magnavox Co.

message. This signal is decoded and the data converted to digital ones and zeros. A block diagram of this function is given in Fig. 54.

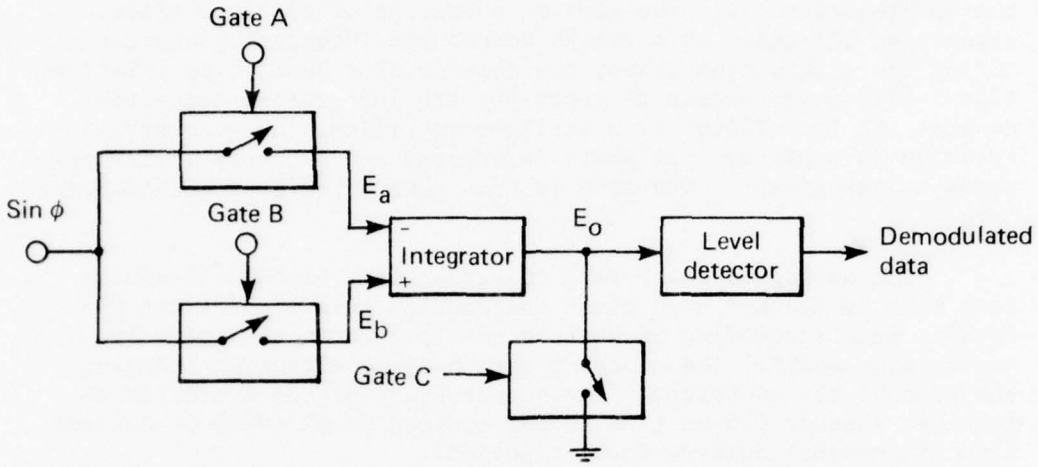


Fig. 54 Block Diagram of the Data Decoder

The sine-phase signal consists of a series of doublets. A positive doublet followed by a negative doublet is by definition a binary one. A negative doublet followed by a positive doublet is a binary zero. Figure 55 shows two data bits and the signals necessary to decode them. In this case, bit synchronization (as described below) has already been obtained and valid data are being decoded.

Doublet rate (DR) and twice doublet rate (2DR) are inputs to a series of flip-flops and gates that generate the signals that control gates A, B, and C, and also the shift pulses. The output of the integrator is at a value of about 6.5 V. Gates A and B are opened and closed in such a pattern that a zero will cause the integrator to go more negative than 6.5 and a one produces an output more positive than 6.5. At the end of a bit, gate C is closed and the integrator is returned to its nominal value of 6.5 V.

The level detector is a voltage comparator that compares the output of the integrator to 6.5 V. Any voltage greater than 6.5 V produces an output at ground. The output of the voltage comparator is clocked into two pairs of flip-flops in series. One

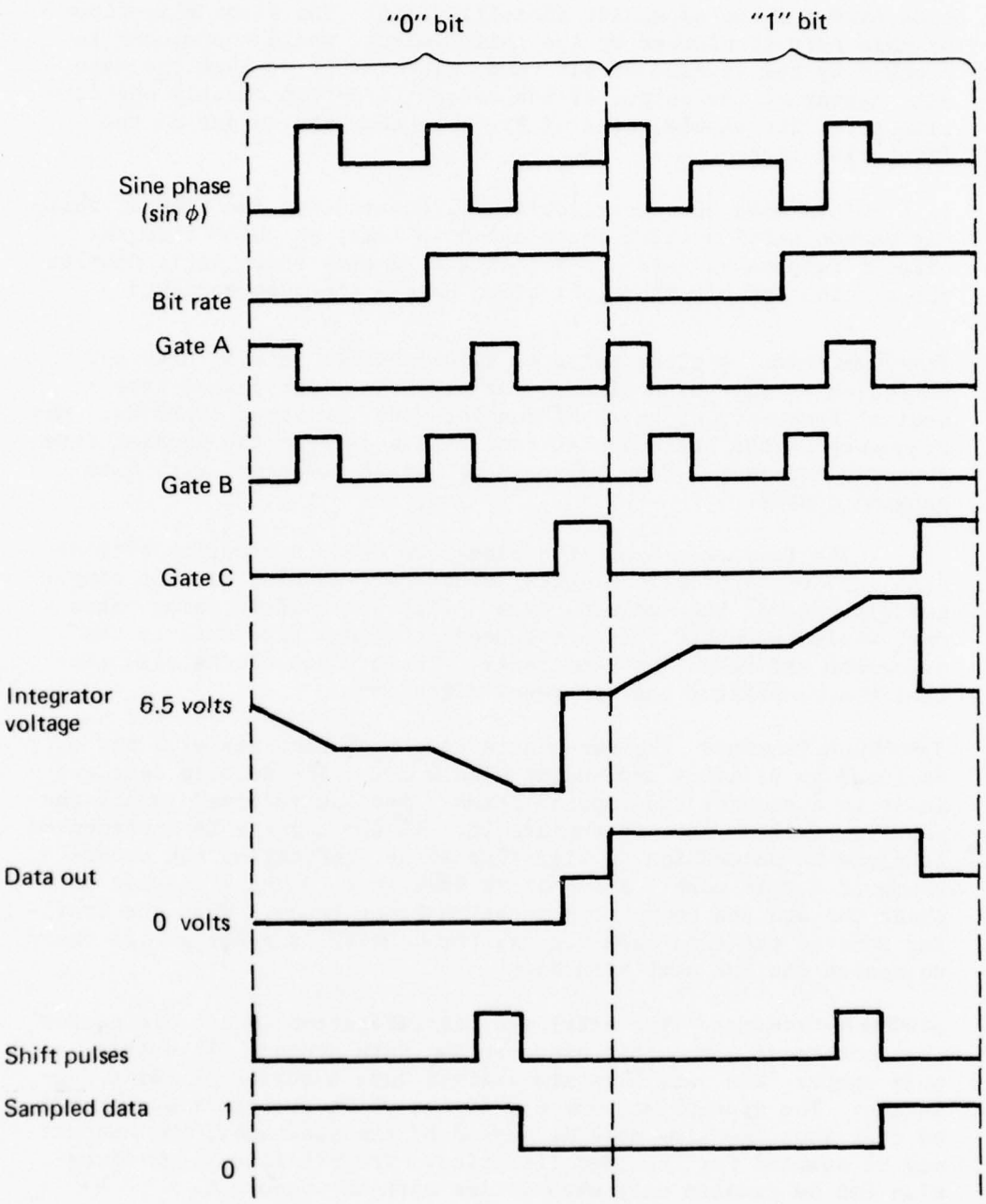


Fig. 55 Decoder Timing and Signal Flow for Full-Bit Decoding

pair is used during the bit-synchronization mode, as described below. The other pair is the input to the logic that extracts the time mark and the satellite identification. The first flip-flop of this pair is clocked by the shift pulses, while the second is clocked by the inverse of bit rate. The result is that the data will appear at the output of the second flip-flop exactly one bit-time late, the sampled data of Fig. 55 being the output of the first flip-flop.

This data decoder circuit will continue to function at full-bit decode until doublet correlation is lost, at which time the circuit returns to half-bit decode and remains there until doublet correlation and bit synchronization have again been achieved.

Four-Phase Clock. A clock pulse of twice doublet rate is used to establish a four-phase clock. The resulting four phases have a nominal frequency of one-half doublet rate, or about 50.85 Hz. The frequency of the half-doublet rate varies as does the doublet rate during phase lock. Each pulse is 2.5 ms in duration, with 5 ms between phases.

The four phases of this clock are used to transfer bits of data into the appropriate gates, since half-doublet rate is simply the bit rate of the incoming data. Bits are shifted using phase one, while the other phases are used to send a time mark to the processor and reset the commutator. These phase clocks also control the commutator and its reset circuitry.

Two-Minute Time Mark. The two-minute time mark consists of a one followed by 23 zeros and ending with a one. The decoded data are input to a counter that counts zeros. Any one received resets the counter, while a zero increments it. If the counter is incremented 23 times in succession, a flip-flop is set indicating the occurrence of a time mark. A signal is then sent to the processor on phase two and the commutator reset on phase three. When the trailing zero of the time mark occurs, the counter is reset and is ready to search for the next time mark.

Satellite Identification. The satellite identification is a 6-bit number that occurs at a specific place in the data stream. To extract this number, the data bits are shifted into a series of shift registers. The appropriate outputs of the shift registers are tapped so that when the time mark is sensed by the processor, the outputs may be sampled for the identification. The satellite identification can be sampled only when a time mark has occurred.

Bit Synchronization (Ref. 2, pp. 7.12 through 7.17). Once doublet correlation has been achieved, the DR is in exact phase and rate synchronization with the doublets being transmitted by the satellite. A bit, however, is composed of two doublets. Therefore, the bit rate is half the doublet rate. In the NMR, a bit rate is generated by dividing doublet rate by two, using a flip-flop. The resulting signal is the same rate as the bits that are being sent by the satellite.

The output of the flip-flop "bit rate" is used with the doublet rate and twice doublet rate to develop the signals that open and close the gates of the data decoder. However, these gate signals may or may not occur at the appropriate time, depending on whether "bit rate" is in phase with the satellite bit rate or 180° out of phase. The result of "bit rate" being 180° out of phase is an inversion of the sampled data. (Figure 56 shows an example of "bit rate" in correct phase.) The purpose of the bit phase synchronization logic is to ensure that "bit rate" is in phase with the satellite bit rate. The bit synchronization process is performed even when "bit rate" is in phase immediately following doublet correlation; the end result is the same.

The sampled data can change states only between bits and not between doublets of the same bit. When "bit rate" is in correct phase, it is a logic one following the decoding of the first doublet of a bit; therefore, a pulse could be generated following a change of state of the sampled data and used to set the "bit rate" flip-flop to a one, as it should be in phase synchronization. This could be done following the first transition of the sampled data if there were no possibility of errors caused by noise.

In order to establish confidence in the validity of the decoding process, a five-stage bidirectional counter is used to count 16 transitions of the sampled data line. The counter is implemented in such a way that it will count up if a transition occurs when "bit rate" is a one, and count down if the transition occurs when "bit rate" is a zero. The counter is reset to the 0111 condition every 80.5 cycles of the 1111 state, and the "bit-rate" flip-flop is set to a one with a pulse from a one-shot. Transitions that occur on the sampled data line because of the transmitted data always occur on the same state of "bit rate," causing the counter to count in the same direction. Transitions that occur on the sampled data line because of noise are as likely to occur when "bit rate" is one as they are when "bit rate" is zero, causing the counter to count up and then back down. If only noise causes transitions on the sampled data line, the counter oscillates around the preset condition and bit sync is not obtained. In this way bit synchronization occurs with a low probability of error.

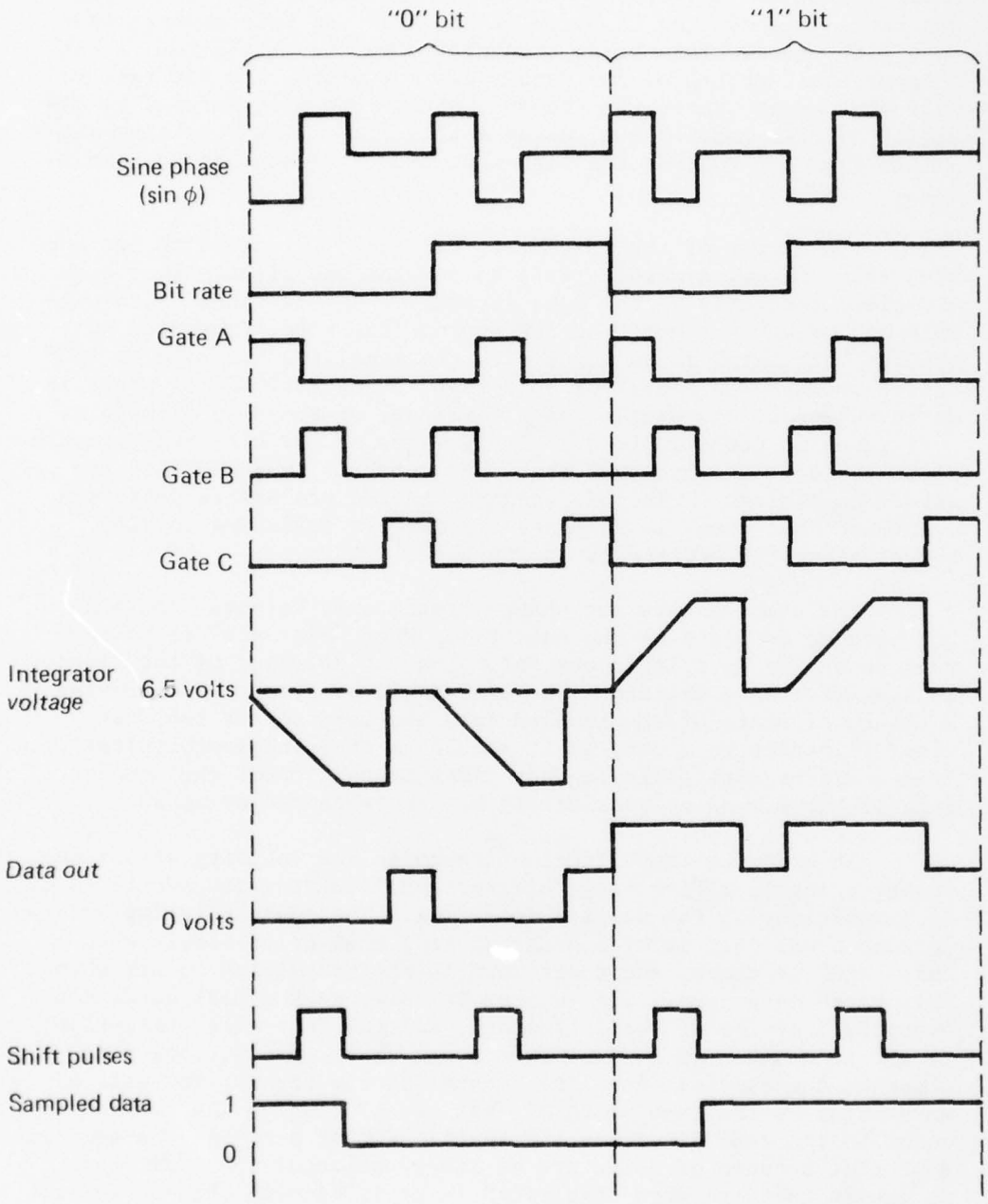


Fig. 56 Decoding of Satellite Data Before Bit Synchronization (bit rate in proper phase)

8. COMMAND SYSTEM INTERFACE

NAVPAC contains no command system per se, but includes magnetic latching relays that interface directly to the HV command system. The 28-V, 100-ms pulses from the HV provide independent on/off power control to the major components of NAVPAC, initiation of a data dump from NAVPAC to the ground tracking stations, and mode-selection controls for the DPU and the PCL electronics. Another interface to a 28-V continuous level (defined as an "HV event") provides information to the tape recorder control logic as to whether or not the recorder can be used for data storage.

9. POWER CONDITIONING UNIT

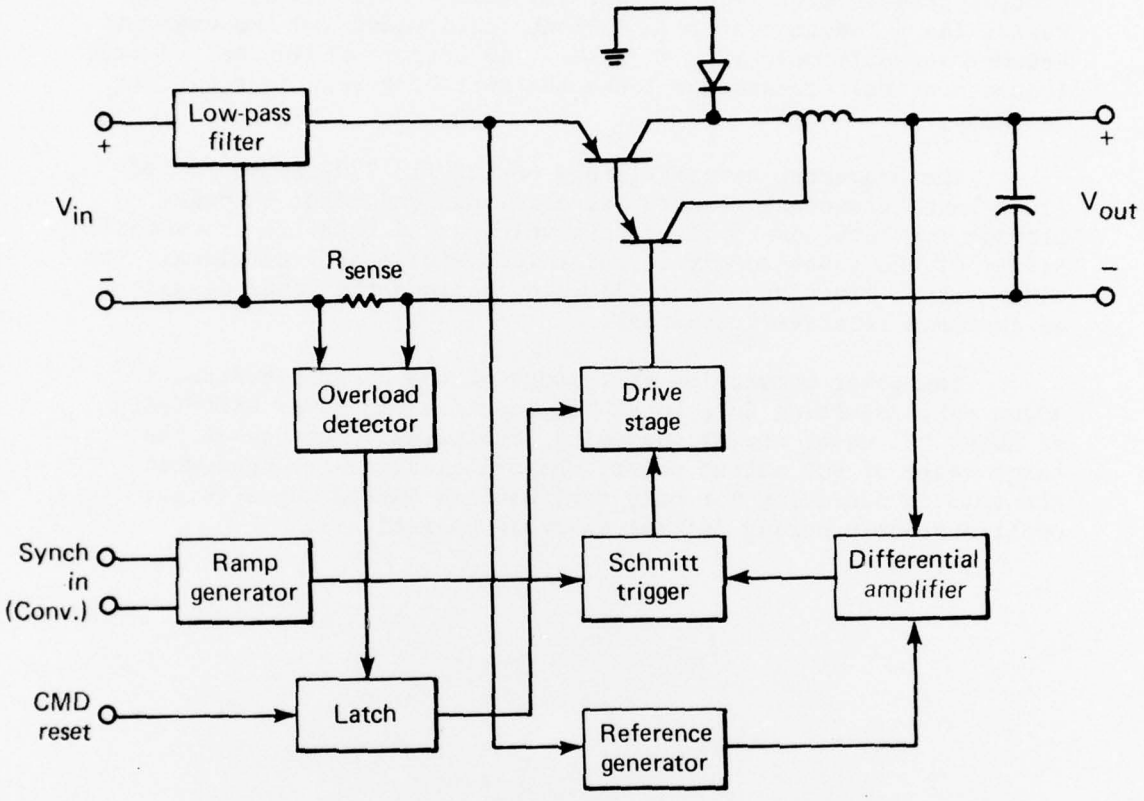
The NAVPAC power conditioning unit (PCU) converts the host-vehicle battery bus into the six regulated DC voltages that are required by the NAVPAC experiment. The PCU consists of a current-limited "buck" switching regulator and a push-pull DC/DC converter.

The input voltage (24 to 33 VDC) to the PCU is processed by the switching regulator to provide a regulated 20 VDC ±1% at its output. This voltage is then converted to AC, rectified, and filtered by the DC/DC converter to provide the regulated output voltages. Output voltage variation on all lines is less than ±5% under all conditions of battery voltage, load current, and baseplate temperature.

PCU output voltages are isolated from the input return while they are referenced to four separate output returns. One set of output voltages (±13 VDC and +5 VDC) is referenced to the main output return, while three fully isolated outputs are provided, two at +5 VDC and one at +6.75 VDC. All output voltages have appropriate EMI filtering.

In addition to providing the regulated output voltages, the PCU functions as an input current limiter for the NAVPAC experiment. Input (battery) current levels exceeding a predetermined threshold result in a crowbar action by the switching regulator, which sets the regulator output voltage (and all PCU outputs) to zero. After removal of the overload condition, the PCU can be reset to its normal mode by command. Should the fault condition remain when the PCU is reset, it will again detect the overload and remove the output voltages. The bus current into the PCU (as well as the PCU output voltages and operating temperature) is monitored by the telemetry system.

The switching regulator (Fig. 57) consists of a pulse width modulator (PWM) controlled by a differential amplifier, a main transistor switch, and an LC output filter. The duty cycle of the constant frequency PWM is controlled in accordance with the basic loop equation (Fig. 57) to provide a constant regulator output voltage. A regulator output voltage exceeding 20 VDC is detected by the differential amplifier, which changes the control signal to the PWM thereby altering the PWM duty cycle. The main transistor switch and its drive stages are controlled by the on/off conduction periods of the PWM. As a result of this switching action, a rectangular voltage waveform is generated at the input of the LC filter.



Basic loop equation: $V_{out} \approx V_{in}\left(\frac{t_{on}}{\tau}\right) - \frac{V_{CE\ (sat)}\ t_{on} + V_{diode}\ t_{off}}{\tau}$

Fig. 57 Equivalent Circuit of the Switching Regulator

Appropriate selection of the filter elements then results in a well-regulated DC output. The regulator bandwidth is approximately 1 kHz and its conversion efficiency is about 93%.

The DC/DC converter (Fig. 58) is a free-running push-pull power oscillator controlled by the saturation characteristics of a control transformer. The nominal switching frequency of 20 kHz varies (as a function of load current requirement and temperature) between approximately 17 and 21 kHz. An output winding on the main (nonsaturating) transformer locks the switching regulator to this frequency.

The converter output filters on the ±13 VDC and +6.75 VDC lines have "frequency corners" at a few hundred hertz in order to provide for both low-ripple output voltage and relative insusceptibility of the power supply to large (dynamic) load variations. The other output lines have less filtering because the power demands on them are relatively constant.

The power conversion efficiency of the DC/DC converter is about 88%, resulting in a total PCU input/output power efficiency of about 82% under normal operating conditions. Because of the large range of PCU output power, the efficiency is reduced when the unit is providing for only very minimal NAVPAC loads (e.g., oscillator-only during initial in-orbit operations).

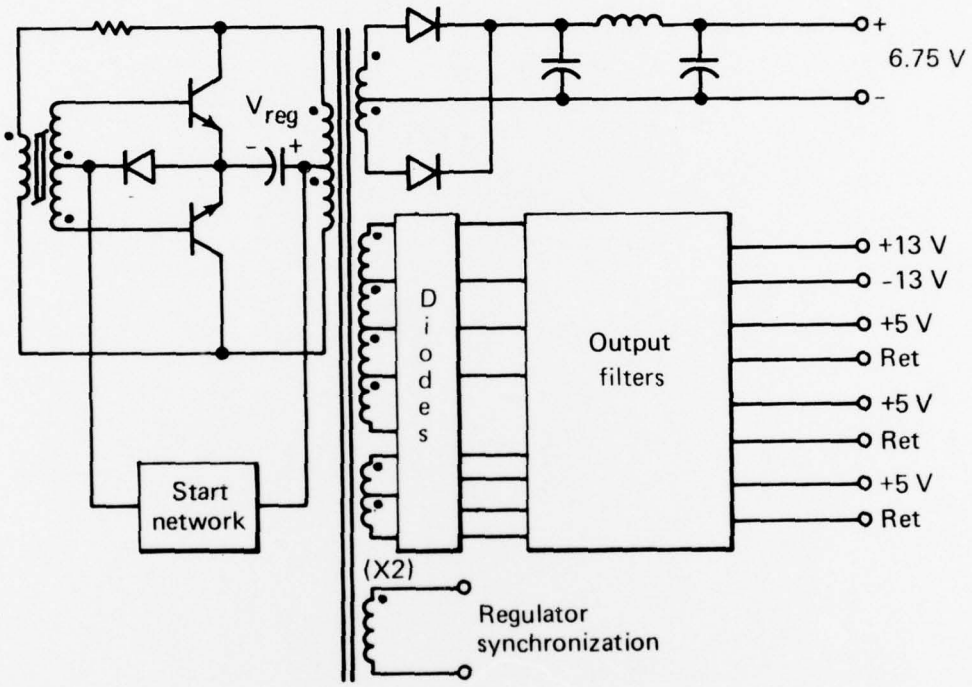


Fig. 58 Equivalent Circuit of the DC/DC Converter

ACKNOWLEDGMENT

Many individuals at the Applied Physics Laboratory contributed to the successful design and development of NAVPAC. Of these individuals, the author gratefully acknowledges the following as contributors to this report.

A. L. Lew
J. C. Loessi
J. R. Norton
P. D. Schwartz
G. R. Seylar
M. W. Shields
R. F. Sloan
S. B. Springer

Appendix A

PHASE DETECTOR ANALYSIS

The phase detectors in the DTL are double-balanced mixers (DBM). The reference signal level is controlled to be large with respect to the input signal, in order to drive the DBM into a switching mode. The output of the phase detector is

$$\text{output volts} = 2\left(\frac{E}{2\pi}\int_{o}^{\pi}\cos(\omega t + \theta)\, d\omega t\right) \qquad \text{(A-1)}$$

$$= \frac{2E}{\pi}\sin\theta,$$

where

E = peak amplitude of the input signal,

θ = phase difference between the input and reference signal, and

ω = frequency in rad/s.

For small angles, $\sin\theta \approx \theta$ in radians; therefore, the phase-detector sensitivity can be written

$$K_2 = \frac{2E}{\pi} \quad \text{V/rad.} \qquad \text{(A-2)}$$

The input impedance of the DBM is 50 Ω. The input power of a signal having a peak amplitude, E, into a 50-Ω load can be expressed in dB above 1 mW (dBm) as

$$\text{dBm} = 10\log\left(\frac{\left(\frac{E^2}{2}\right)\left(\frac{1}{50}\right)}{1 \times 10^{-3}}\right) = 10\log\left(\frac{\text{input power}}{1\text{ mW}}\right), \qquad \text{(A-3)}$$

$$= 10\log 10E^2. \qquad \text{(A-4)}$$

Solving for E in terms of dBm,

$$\frac{dBm}{10} = \log (10E^2) \tag{A-5}$$

$$10E^2 = 10^{\frac{dBm}{10}} \tag{A-6}$$

$$3.16E = 10^{\frac{dBm}{20}} \tag{A-7}$$

$$E = 0.316 \left(10^{\frac{dBm}{20}}\right) \tag{A-8}$$

Substituting Eq. A-8 into Eq. A-2 gives:

$$K_2 = \frac{2}{\pi} \left[0.316 \left(10^{\frac{dBm}{20}}\right) \right] \tag{A-9}$$

$$= 0.201 \left(10^{\frac{dBm}{20}}\right) \text{ V/rad.} \tag{A-10}$$

Equation A-10 represents the theoretical sensitivity of the phase detector. In actual design procedures, the dBm value in the equation must be modified to include about a 1-dB insertion loss of the DBM.

Consider the following example where the input power = 0 dBm.

$$K_2 = 0.201 \left(10^{\frac{0}{20}}\right) = 0.201 \text{ V/rad} \quad \text{(theoretical value)}$$

$$K_2 = 0.201 \left(10^{\frac{0-1}{20}}\right) = 0.179 \text{ V/rad} \quad \text{(practical value)}$$

Appendix B

CLOSED-LOOP AGC ANALYSIS

Figure B-1 describes a closed-loop gain control system designed to maintain a constant signal level at the output of the IF amplifier by varying the attenuation of the VCA as the input signal varies in amplitude.

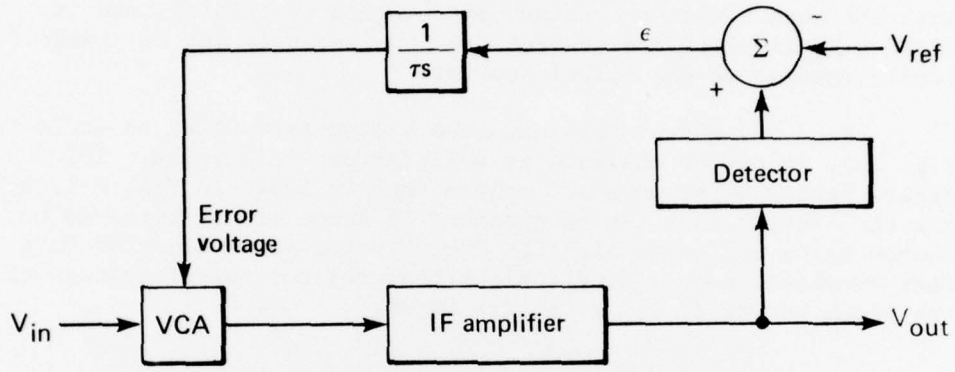


Fig. B-1 Closed-Loop Gain-Control System

In Fig. B-1

VCA ≡ log attenuator having a gain constant = A (dB/V).

IF amplifier ≡ linear device having a $\frac{\Delta \text{ signal out}}{\Delta \text{ signal in}}$ gain constant = dB/dB = 1. In other words, a 1-dB increase at the input corresponds to a 1-dB increase at the output.

Detector ≡ amplitude detector whose output is linear with input (AC input, DC output) and whose output is to be regulated to a value = V_{ref}. Input and output are volts, therefore the gain in dB/dB is unity. In other words, a 1-dB increase at the input results in a 1-dB increase at the output.

$\Sigma \equiv$ "subtractor" that provides the difference between the detector output and the reference. Input and output are volts; however, it is desired that the transfer function of the subtractor be (volts out)/dB in. In other words, the device must act as a subtractor and a translator of volts input to dB input.

$\frac{1}{\tau s} \equiv$ loop network to obtain the desired regulator response. Input and output are in volts/volt or dB/dB.

When the analysis of Fig. B-1 is started, it soon becomes apparent that a more convenient model would be helpful, and it would also simplify the analysis to consider only the dB change in levels instead of the actual levels.

Katz has shown* that when the system is modeled as it is in Fig. B-2, it can be analyzed as a linear control system. This figure presents the same AGC system that is shown in Fig. B-1, but now the control loop can be examined in terms of dB increases or decreases in the input signal. The detector and subtractor have been represented by a single block that relates output voltage of the block to the dB change at its input.

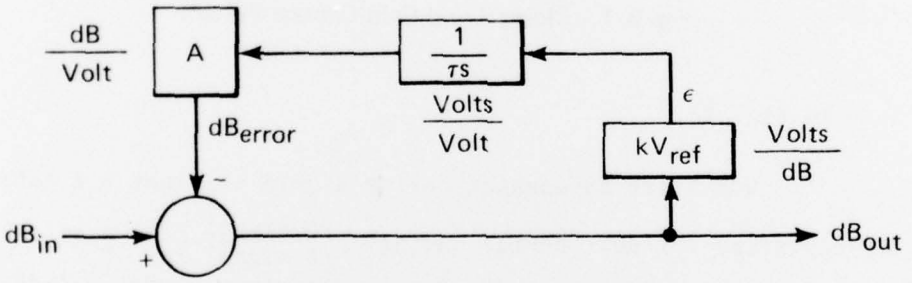


Fig. B-2 Equivalent Circuit of Closed-Loop Gain Control

For the analysis of the subtractor-translator refer to Fig. B-3, which defines the inputs and output of the subtractor.

* Correspondence from Mr. L. Katz of the Electrac Corp., Anaheim, CA, July 1974.

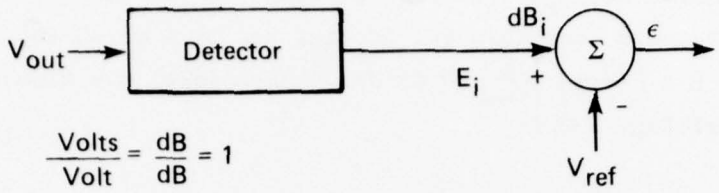


Fig. B-3 Inputs and Outputs of the Subtractor-Translator

$$dB_{in} = 20 \log \frac{E_i}{V_{ref}} = 20 \log \frac{E}{V} \, dB, \qquad \text{(B-1)}$$

or

$$E = V10^X \quad \text{where } X = \frac{dB_{in}}{20} .$$

$$\epsilon = V10^X - V = V(10^X - 1) . \qquad \text{(B-2)}$$

For $X < 1$

$$10^X - 1 = 2.302X + \frac{(2.302X)^2}{2!} + \ldots ,$$

and for $X \ll 1$

$$10X - 1 \approx 2.302X = 2.302\left(\frac{dB_{in}}{20}\right).$$

Therefore,

$$\epsilon \text{ volts} \approx \left[2.3\left(\frac{dB_{in}}{20}\right)\right] V = \left[\frac{V_{ref}}{8.68}\left(\frac{volts}{dB}\right)\right] dB_{in} \quad \text{(in dB)} . \qquad \text{(B-3)}$$

The transfer function can now be expressed in terms of the input signal changes in dB and V_{ref}.

As an example, if V_{ref} = 5 volts and the VCA constant = 10 dB/volt, then the forward loop gain (G) of Fig. B-2 is 1 dB/dB and the feedback loop $H = \left(\frac{5}{8.68}\right)\left(\frac{1}{\tau s}\right) 10$ dB/dB . Therefore, the closed-loop response of Fig. B-2 is

$$\frac{G}{1 + GH} = \frac{dB_{out}}{dB_{in}} = \frac{1}{1 + \frac{50}{8.68\tau s}} = \frac{s}{s + \frac{5.76}{\tau}} . \qquad \text{(B-4)}$$

The closed-loop response of the AGC system is therefore a high-pass function with a corner frequency of $5.76/\tau$ radians per second. Selection of the corner frequency is influenced by signal dynamics as well as the characteristics of the AC signal that exist at the input to the AGC system because of the modulation. The system must be able to respond to variations in signal strength, but must not respond so fast as to destroy the modulation.

The NAVSAT phase modulation of 0°, +60°, and -60° results in the presence of a 101.7-Hz square wave at the output of the AGC detector. The output of the auxiliary phase detector (the detector used for the AGC system) is cosine 0°, cosine +60° and cosine -60°, and is shown in Fig. B-4.

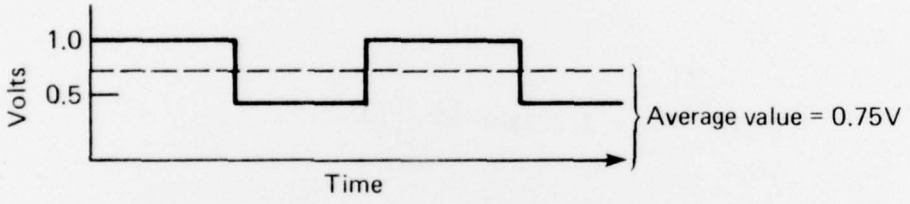


Fig. B-4 Output from the Phase Detector

The "up" excursion error = $20 \log \frac{1}{0.75}$ = 2.5 dB. The "down" excursion error = $20 \log \frac{0.75}{0.5}$ = 3.5 dB. Therefore the average excursion of the AC signal around the average DC value is 3 dB.

The AGC error response of Fig. B-2 is

$$\frac{dB_{error}}{dB_{in}} = \frac{dB_{in} - dB_{out}}{dB_{in}} = 1 - \frac{dB_{out}}{dB_{in}}$$

$$= 1 - \frac{s}{s + \frac{5.76}{\tau}} = \frac{\frac{5.76}{\tau}}{s + \frac{5.76}{\tau}} \quad . \qquad \text{(B-5)}$$

The error response is seen to be a low-pass function. As an example, if it is decided that the maximum error at 100 Hz caused by the feedback of the AGC system is to be 0.2 dB, then the error response must provide an attenuation of 3.0/0.2 = 15. Because the slope of the low-pass error function is 6 dB/octave, the low-pass corner can be adjusted as

$$\frac{5.76}{\tau} = \frac{2\pi(100)}{15} = 42 \text{ rad/s} = 6.67 \text{ Hz.}$$

The parameters of the loop network can now be selected from

$$\frac{5.76}{\tau} = 42 \rightarrow \tau = RC = 0.14 \text{ s.}$$

Note that τ is a parameter of the loop network and is not the AGC time constant. For this example, the AGC time constant, T, is

$$T = \frac{\tau}{5.76} = 0.024 \text{ s.}$$

INITIAL DISTRIBUTION EXTERNAL TO THE APPLIED PHYSICS LABORATORY*

The work reported in TG 1317 was done under Navy Contract N00017-72-C-4401. This work is related to Task ZA8, which is supported by Defense Mapping Agency.

ORGANIZATION	LOCATION	ATTENTION	No. of Copies
DEPARTMENT OF DEFENSE			
DDC	Alexandria, VA		12
Department of the Navy			
Headquarters			
NAVSEASYSCOM	Washington, DC	PMS 395A1	1
		SEA-09G3	2
NAVPRO	Laurel, MD		1
CNO	Washington, DC	OP-986F	2
		OP-09	1
		OP-212	2
CNM	Washington, DC	NMAT 0323E	1
Strategic Systems Project Office	Washington, DC	SP-24	1
		SP-25	1
Naval Electronic Systems Command	Washington, DC	NAVELEX 520	2
		PME-106-21	1
		PME-106-22	1
Centers			
NSWC	Dahlgren, VA	Code DK-13	1
		Everett Swift	1
		Robert Hill	1
Navy Astronautics Group	Point Mugu, CA		5
Department of the Air Force			
Air Force Geophysics Laboratory	Bedford, MA	AFGL	1
U.S. GOVERNMENT AGENCIES			
Defense Mapping Agency, HQ	Washington, DC	Adv. Tech. Division	1
		Dr. C. F. Martin	3
Defense Mapping Agency, TC	Washington, DC	Code 52310	1
		Code 52200	1
		Code 52400	1
National Aeronautics & Space Admin., Goddard Space Flight Center	Greenbelt, MD	Dr. David E. Smith, Code 921	1
		Dr. F. O. Vonbun, Code 900	1
		Dr. Joseph W. Siry, Code 900	1
CONTRACTORS			
Lockheed Missiles & Space Co.	Sunnyvale, CA	William Hamada	1
		Will L. Carr	1
		George Clapp	1

Requests for copies of this report from DoD activities and contractors should be directed to DDC, Cameron Station, Alexandria, Virginia 22314 using DDC Form 1 and, if necessary, DDC Form 55.

*Initial distribution of this document within the Applied Physics Laboratory has been made in accordance with a list on file in the APL Technical Publications Group.